

**Engineering and Technical Services
for Joint Group on Pollution
Prevention (JG-PP) Projects**

Joint Test Report

CC-R-1-1

**for Validation of Alternatives to Lead-Containing
Surface Finishes, for Development of Guidelines for
Conformal Coating Usage, and for Qualification of
Low-VOC Conformal Coatings**

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PREFACE

The National Defense Center for Environmental Excellence (NDCEE) operated by Concurrent Technologies Corporation (CTC), prepared this report under Contract Number DAAE30-98-C-1050. This report was prepared on behalf of and under guidance provided by the Joint Group on Pollution Prevention (JG-PP) through JG-PP Working Group (JWG). The structure, format, and depth of technical content of the report were determined by the JWG, government contractors, and other government technical representatives in response to the specific needs of this project.

We wish to thank the participants involved in the creation of this document for their invaluable contributions.

- Advanced Medium Range Air-to-Air Missiles (AMRAAM) Program Office
- Aeronautical System Center/Environmental Management (ASC/EM), Wright Patterson Air Force Base (AFB)
- AIM-9X Program Office
- Air Force Corrosion Program Office
- AMSAM-DSA-SH-PTC
- Avenger Program Office
- C-17 Program Office
- Circuit Card Assembly and Materials Task Force (CCAMTF)
- Defense Contract Management District - West (DCMDW-OS)
- ESC/EN-IB, Hanscom AFB, MA
- F-15 Program Office
- F-16 Program Office
- F-22 Program Office
- Head Quarters Air Force Materiel Command/Logistics Group-Environmental (HQ-AFMC/LG-EV), Wright Patterson AFB
- HQ Army Aviation and Missile Command (AMCOM)
- HQ Defense Contract Management Agency (DCMA)
- Javelin Program Office
- Joint Stand Off Weapon (JSOW) Program Office
- M1 Abrams Program Office
- Major Command (U.S. Army)
- National Aeronautics and Space Administration (NASA) Aerospace Materials Division
- Naval Air Warfare Center (NAWC) – Weapons Division
- Naval Surface Warfare Center (NSWC) - Crane Division
- Office of Chief of Naval Operations (CNO), Environmental Protection, Safety, and Occupational Health
- Phalanx Program Office
- RAM Program Office
- Robisan Laboratory, Incorporated
- Short-Range Air Defense (SHORAD)
- Sidewinder Program Office
- Standard Missile Program Office
- Stinger Program Office
- Tank-Automotive and Armament Command (TACOM) – Army Armament Research and Development Energy Center
- Tomahawk Program Office
- Trident Program Office
- U.S. Army HQ-Communications Electronics Command (CECOM)

- Volcano Program Office
- Warner Robins Air Logistic Center (WR-ALC)/LFEFA, Robins AFB
- WR-ALC, Robins AFB
- Wright Laboratories, Wright Patterson AFB
- U.S. Army PEO-TAD

EXECUTIVE SUMMARY

The Circuit Card Assembly and Materials Task Force (CCAMTF) was formed in September 1995 to develop and conduct a joint test program for evaluating the reliability of new manufacturing technologies and materials used in the production of circuit card assemblies. The CCAMTF is a consortium of 22 industry, military, and government organizations funded by the 22 participants and by the Joint Group on Pollution Prevention (JG-PP). (See Appendix A for a complete list of individual participants and their organizations.)

The CCAMTF determined that many of the materials on the MIL-I-46058 Qualified Product List had volatile organic compound (VOC) levels that exceeded new federal and regional regulatory limits. For example, surface finishes containing tin and leads are applied to circuit cards to prevent oxidation of exposed copper. Lead is a toxic substance that is now heavily regulated by various federal, state, and local environmental agencies. To address new environmental concerns such as this, the CCAMTF was to determine whether new technologies and materials could effectively replace certain hazardous processes or hazardous materials (HazMats) used to manufacture and maintain state-of-the-art, performance-on-demand military and high-end commercial electronics. Successful replacement could abate potential environmental safety and occupational health risks and could favorably impact manufacturing costs.

The CCAMTF formulated the following goals for its test program.

1. Qualification of lead-free organic and metallic printed wiring assembly (PWA) surface finishes
2. Validation of guidelines for intelligent use of conformal coating
3. Qualification of low-volatile organic compound (VOC) conformal coatings.
Low-VOC is defined as less than 420 grams (g) of VOC/ liter of mixed coating (3.5 pounds per gallon).

Prior to testing, a joint group led by the JG-PP Working Group (JWG), the CCAMTF, and the National Defense Center for Environmental Excellence (NDCEE) identified engineering, performance, and operational impact (supportability) requirements for circuit cards prepared both with and without conformal coatings and with various lead-free surface finishes. The joint group selected these conformal coatings for testing: parylene, silicone, urethane, and uncoated. Benzimidazole, Immersion Gold (Au), and Immersion Silver Palladium (Ag/Pd) were the lead-free surface finishes chosen along with a baseline surface finish of tin lead (Sn/Pb) Hot Air Solder Leveling (HASL). The joint group also chose to test both a water-soluble and low-residue flux. The joint group reached consensus regarding tests to qualify alternatives against the requirements, including procedures, methodologies, and acceptance criteria.

Circuit cards prepared by the American Competitive Institute are referred to as PWA test vehicles throughout this report. Each PWA contained 23 circuits that had been prepared with each of the surface finishes under study (three alternative surface finishes, three conformal coatings and two fluxes). In this way, all surface finishes under study were simultaneously

exposed to such variables as diesel fuel, hydraulic fluid, branch water, humidity, and thermal shock.

This Joint Test Report (JTR) documents the validation testing results for the three alternative surface finishes, the three conformal coatings, and two fluxes chosen for study by the CCAMTF. Test results were summarized below.

Diesel Fuel and Hydraulic Fluid

After exposing the PWA to diesel fuel and hydraulic fluid, the test sequence statistical analysis showed no relationship between surface finish and performance. Conformal coating was determined to provide no benefit to the 23 circuits contained on the PWA.

Branch Water Test

Performance did not differ significantly for alternative surface finishes during the branch water test. The results for conformal coating showed that parylene and urethane slightly outperformed silicone; uncoated PWAs had significantly more anomalies than conformal coated PWAs.

Salt Fog Test

Following 500 hours of exposure to salt fog, testing was unable to be performed since the Joint Test Protocol (JTP) did not call out any masking specifications and the PWAs were too severely corroded for the Automated Test Set (ATS) to perform electrical testing.

Humidity and Thermal Shock Testing

Following exposure to 85°C/85% humidity and thermal shock testing, it was determined that no statistical differences could be noted among surface finishes or conformal coatings.

Exposure to Condensing-Atmosphere and Thermal-Cycling Tests

Alternative surface finishes again showed no significant differences in performance upon completion of the condensing-atmosphere and thermal-cycling tests. There were, however, notable differences in the performance of the conformal coatings; parylene and silicone outperformed both urethane and uncoated PWAs.

Accelerated Life-Vibration, Mechanical-Shock, Branch-Water Testing

Upon completion of the accelerated life-vibration, mechanical-shock, branch water testing sequence, it was again found that no significant differences could be identified between surface finishes. It was determined that the parylene conformal coating outperformed silicone and urethane. Uncoated PWAs performed poorly.

Flux Type

In all testing, it was determined that flux type played no role in the performance of the PWAs with respect to the JTP acceptance criteria.

High-Voltage Circuits in High-Humidity Environments

Upon completion of the CCAMTF testing schedule, it was found that a performance improvement was provided when applying conformal coating (vs. no conformal coating) for

high-voltage circuits in high-humidity environments (i.e. branch water, salt fog, and condensing atmosphere). Parylene statistically appeared to perform better than silicone, which outperformed urethane in the condensing atmosphere/thermal cycling and salt fog test sequences. However, all conformal coatings outperformed uncoated PWAs in these tests. The effects appeared to be reversed once the PWAs were dried and retested. Surface finishes appeared to have little effect under these conditions with the exception of benzimidazole, which failed to meet the JTP acceptance criteria.

Low-Voltage Circuits

For low-voltage circuits there were no detectable statistical differences between surface finish, conformal coating, and flux type.

Conclusion

Conformal coatings are usually applied to circuit cards to protect against adverse conditions such as those used as test variables by the CCAMT. Conformal coatings can be expensive to apply and in some instances are the sources of up to 40 percent of VOCs produced in high-volume manufacturing operations. A reduction in the use of conformal coatings could decrease manufacturing costs, simplify rework, and reduce pollution at the source. This CCAMTF study shows that it is debatable whether the additional cost incurred to apply conformal coating can be justified under many of the environmental conditions tested. This is not to say that conformal coating would not prove to be beneficial for some circuits in some cases, but that it did not appear to play a significant role in determining which PWAs met the acceptance criteria set forth in the JTP. It is recommended that any changes regarding conformal coating use and application of surface finishes be reviewed on a case-by-case basis.

1. INTRODUCTION

The Joint Logistics Commanders (JLC) and Headquarters National Aeronautics and Space Administration (NASA) co-chartered the Joint Group on Pollution Prevention (JG-PP) to coordinate joint service/agency activities affecting pollution prevention issues identified during system and component acquisition and sustainment processes. The primary objectives of the JG-PP are to:

- Reduce or eliminate the use of hazardous materials (HazMats) or hazardous processes at manufacturing, remanufacturing, and sustainment locations
- Avoid duplication of effort in actions required to reduce or eliminate HazMats through joint service cooperation and technology sharing.

JG-PP projects typically involve at least one original equipment manufacturer (OEM) producing multiple systems for more than one of the Services or NASA, as well as at least one facility, such as a Department of Defense (DoD) depot, maintaining one or more of the systems. JG-PP technical representatives for each project begin by selecting at least one target HazMat for reduction or elimination. This target HazMat(s) is a material used in production or sustainment processes that is known to create environmental and/or worker health concerns. Project participants then identify alternative technologies or materials for evaluation.

For each project, a Joint Test Protocol (JTP) is written, containing the critical requirements and tests necessary to qualify potential alternatives to selected target HazMats and processes for a particular application. The required tests for this project are documented in *Joint Test Protocol, CC-P-1-1, Validation of Alternatives to Lead-Containing Surface Finishes, for Development of Guidelines for Conformal Coating Usage, and for Qualification of Low-VOC Conformal Coatings*, dated June 23, 1999, hereafter referred to as JTP. The testing requirements are summarized in Section 2.

During each project, the participating technical representatives select candidate alternatives that will be tested in accordance with the JTP. The alternatives are listed in Section 3.

After project participants define the tests to be performed and the alternatives to be tested, testing is executed. This Joint Test Report (JTR) documents the results of the testing, describes any test modifications made during the execution of testing, and identifies technically acceptable alternatives to the baseline process. Any test procedure modifications documented in this JTR have been agreed upon by the project technical stakeholders.

For the Lead-Free Surface Finishes and Low-Volatile Organic Compound (VOC) Conformal Coatings project, lead and VOCs as found in surface finishes and conformal coatings respectively were identified as the target HazMats to be eliminated or reduced.

This JTR will be made available as a reference for future pollution prevention efforts by other DoD, NASA, and commercial users to minimize duplication of effort.

1.1. CCAMTF Overview

The Circuit Card Assembly and Materials Task Force (CCAMTF) is a consortium of industry, military, and government organizations whose purpose is to identify alternative materials and processes that have the potential to abate environmental, safety, and occupational health (ESOH) risks; reduce costs; and improve efficiency when compared to current methods of circuit card manufacturing and maintenance. Appendix A lists the organizations and their representatives that participate in the CCAMTF.

The CCAMTF is currently implementing initiatives that have significant potential to provide pollution prevention, cost, and production efficiency benefits. These initiatives include:

- Demonstrating and validating lead-free organic and metallic surface finishes
- Developing guidelines for intelligent use of conformal coatings
- Demonstrating and validating low-VOC conformal coatings.

Surface finishes containing tin and lead are applied to circuit cards to prevent oxidation of exposed copper. This application ensures a solderable surface when components are added during later stages of processing. The most widely used processes for applying solder alloy surface finishes are hot-air solder leveling (HASL) and reflowed tin-lead. HASL can be used on boards with or without solder mask present. Both processes generate lead emissions and waste. Lead is a toxic substance that is heavily regulated by various federal, state, and local environmental agencies.

A related concern for fused tin-lead surface finishes is their inability to provide a level soldering surface. Planarity is extremely important in the reliable placement and soldering of fine pitch components. Tin-lead surface finishing is seen as a limiting technology in this respect. The CCAMTF believes that lead-free alternative surface finishes would provide increased planarity.

Conformal coatings are thin layers of synthetic resins or polymers applied to circuit cards for protection against a variety of environmental, mechanical, electrical, and chemical conditions; these conditions include humidity, moisture, contamination, stress, mechanical shock, vibration, thermal cycling, and corrosion. The application process is expensive, and time consuming, and also accounts for up to 40% of the VOC emissions generated from high-volume circuit card manufacturing. (The remaining 60% of VOC emissions is generated by soldering fluxes, primers, and cleaning agents.) VOC emissions are heavily regulated by various federal, state, and local environmental agencies.

The CCAMTF believes that intelligent use of conformal coatings would decrease manufacturing costs, simplify rework, and reduce pollution at the source without degrading circuit card quality or performance. Guidelines for intelligent use of conformal coatings would describe suitable applications that reduce the use of conformal coatings, use low-VOC conformal coatings, or use conformal coatings without primers.

Table 1 summarizes the target HazMat, current processes, applications, and current specifications. Table 2 contains the defense systems programs potentially affected by the CCAMTF/JG-PP project and this JTR.

Table 1. Target HazMat Summary

Target HazMats	Current Processes	Applications
Lead	Surface Finishing	Oxidation Protection
VOCs	Conformal Coating	Corrosion Protection, Electrical Insulation, and Foreign Object Debris (FOD) Protection
Current Specifications		
ANSI/J-STD-001	IPC-D-275	MIL-PRF-31032
IPC-6011	IPC-SM-782	MIL-S-45743
IPC-6012	IPC-RB-276	MIL-STD-275
IPC-2221	IPC-RF-245	MIL-STD-454
IPC-2222	MIL-C-28809	MIL-STD-2000
IPC-CC-830	MIL-I-46058	MIL-STD-2000A
IPC-CM-770	MIL-P-50884	MIL-STD-2118
IPC-D-249	MIL-P-55110	WS6536

Table 2. Potentially Affected Defense System Programs

Potentially Affected Defense Systems
Air Force
AGM-65 Maverick Missile System
APQ-181 (B-2 Radar)
B-2 Spirit Bomber Aircraft
C-17 Globemaster III Transport Aircraft
C130J Hercules Transport Aircraft
C-141B Starlifter Transport Aircraft
Design, Evaluation for Personnel, Training, and Human Factors (DEPTH)

(Table 2 continued on next page)

Table 2. Potentially Affected Defense System Programs (continued)

Potentially Affected Defense Systems
Air Force (continued)
F-15 Eagle Fighter Aircraft
F-16 Fighting Falcon Fighter Aircraft
F-22 Air Superiority Fighter Aircraft
GBU-15 Glide Bomb
High Power Microwave Suppression of Enemy Air Defenses (HPM SEAD)
KC-10A Extender Tanker Aircraft
Solid-State Phased Array (SPAR) Radar System
Army
Advanced Tank Armament System (ATAS)
Avenger Missile System
CH-47 Chinook Transport Helicopter
Cobra-NITE/LAAT Targeting System
FIREFINDER Position Analysis System
Gunner's Primary Sight-Line of Sight (GPSLOS)
Horizontal Technology Integration (HTI) Targeting System
Improved Bradley Acquisition System (IBAS) Targeting System
Improved Target Acquisition System (ITAS) Targeting System
Javelin Missile System
Lightweight Exo-Atmospheric Projectile (LEAP)
M1A2 Abrams MBT CITV/HTEU
M65 TOW Targeting System
M139 VOLCANO Mine Dispensing System
M732A2 Fuze
M762 Fuze
M773 MOFA Fuze
OH-58 Kiowa Transport Helicopter
PALADIN Howitzer Fire Control
Stinger Missile System
Standard Vehicle Mounted Launcher (SVML)
Target Acquisition Designation Sight/Pilot Night Vision Sensor (TADS/PNVS)
TOW 2A & 2B Missile Systems
XM943 Smart Target Activated Fire and Forget (STAFF) Tank Ammunition Round
Navy
AGM-84E SLAM Missile System
APG-73 Radar System
AV-8 Harrier VTOL Attack Aircraft
CIWS Phalanx Weapon System
Evolved SeaSparrow Missile (ESSM) Missile System

(Table 2 continued on next page)

Table 2. Potentially Affected Defense System Programs (continued)

Potentially Affected Defense Systems
Navy (continued)
F/A-18 Hornet Fighter/Attack Aircraft
Guided Missile Launching System (GMLS)
HH-60 Seahawk Helicopter
Mk612 Standard Missile Test Set
P-3 Orion Synthetic Aperture Radar (SAR)
Rolling Airframe Missile (RAM)
SH-60F CV-Helo ASW Helicopter
SLBM Trident I-C4 & II D-5 Missile System
SM-1, SM-1A & SM-2 Standard Missile Systems
Tomahawk Baseline Improvement Program (TBIP)
Tomahawk Missile System
Joint/Multi-Service Systems
AGM-84D Harpoon Missile System
AIM-9X Sidewinder Missile System
AIM-120 AMRAAM Missile System
AGM-88 HARM Missile System
F-3 Tornado Fighter Aircraft
Integrated Targeting System Gun Management System (ITSGMS)
Joint Air To Surface Standoff Missile (JASSM)
Joint Stand-Off Weapon (JSOW) Missile System
Joint Strike Fighter (JSF) Fighter Aircraft
LAMPS/FLIR Targeting Systems
LANTIRN Targeting System
Objective Individual Combat Weapons (OICW) Weapon System
Outrider Tactical Unmanned Air Vehicle (TUAV)
Paveway III Missile System
V-22 Osprey VTOL Transport Aircraft

2. TESTING REQUIREMENTS

The following sections summarize the validation testing requirements for the printed wire assemblies (PWAs) prepared with and without conformal coatings, with various lead-free surface finishes, and with either low residue flux (LR) or water soluble flux (WS). The PWA chosen for testing was adopted from the Low-Residue Soldering Task Force (LRSTF). A description of the PWA that had been chosen by the CCAMTF can be found in Section 2.1 of this JTR. Appendix B contains a detailed description of the LRSTF PWA.

In the LRSTF project, each electrical response from the LRSTF PWA was manually tested, which required two technicians to each spend approximately 30 minutes on each PWA. In addition to being time consuming, the CCAMTF was concerned with measurement variability introduced through the use of different technicians at different test times. In view of these concerns and the large number of PWAs to be tested, the CCAMTF decided to design an Automated Test Set (ATS) to perform automatic testing of the LRSTF PWA. Raytheon in McKinney, Texas, designed the CCAMTF ATS. A description of the ATS can be found in Section 2.2 of this JTR.

Tests were conducted in a manner that eliminated duplication and maximized use of each test specimen. For example, where possible, more than one test was performed on each specimen. The amount and type of tests that were run on any one specimen were determined by the destructiveness of the test. A test flow diagram has been included as Figure 2 in Section 2.4 of this JTR to illustrate the sequence and phases of testing.

The testing requirements presented in this section and subsequent sections of this report were carried out in three individual phases. The first of these phases was that of a screening phase described in Section 4.1 of this JTR. From this screening phase, and the data it provided, alternative surface finishes and conformal coatings were chosen. These alternatives were then exposed to the validation portion of the testing. The validation portion was divided into two individual phases. The first of which was environmental exposure testing (Phase I), and the second of which was physical reliability testing (Phase II).

Table 3 and Table 4, respectively, in Section 2.3 list the environmental exposure and physical reliability validation testing requirements identified by the CCAMTF project participants for validating alternatives to lead-containing surface finishes, and VOC containing conformal coatings. The listings in Table 3 and Table 4 include acceptance criteria and the references, if any, used for developing the tests. Overviews for each of the environmental exposure and physical reliability validation tests can be found in Section 4.4 and Section 4.5 respectively of this JTR. For full testing descriptions please reference Section 3.4 and Section 3.5 of the JTP.

2.1. Printed Wiring Assembly

The PWA is a test circuit assembly used to evaluate a variety of electrical performance parameters. It was designed to represent the majority of parts produced for military applications, and to accurately reflect relative differences in alternative surface finish and conformal coating performance. The PWAs utilized in the testing documented throughout this JTR were assembled at the American Competitiveness Institute (ACI) in Plymouth Meeting Pennsylvania. The PWA measures 6.05 inches by 5.8 inches by 0.062 inches, and contains the following six sections:

- High current, low voltage (HCLV)
- High voltage, low current (HVLC)
- High speed digital (HSD)
- High frequency (HF)
- Other networks (ON)
- Stranded wire (SW).

Each section of the PWA has independently performing subsections for plated through hole (PTH) and surface mount technology (SMT) components. Each subsection (except the SW section) contains both functional and nonfunctional components (added to increase component density). A 29-pin PTH edge connector is used for circuit testing. High frequency connectors are used to ensure proper impedance matching and test signal fidelity. Two stranded wires are soldered to terminals on the board. The PWA includes a common ground plane, components with heat sinks, and mounted hardware. Appendix B of the JTP contains a detailed description of the Low-Residue Soldering Task Force (LRSTF) PWA. The layout of the PWA is shown in Figure 1.

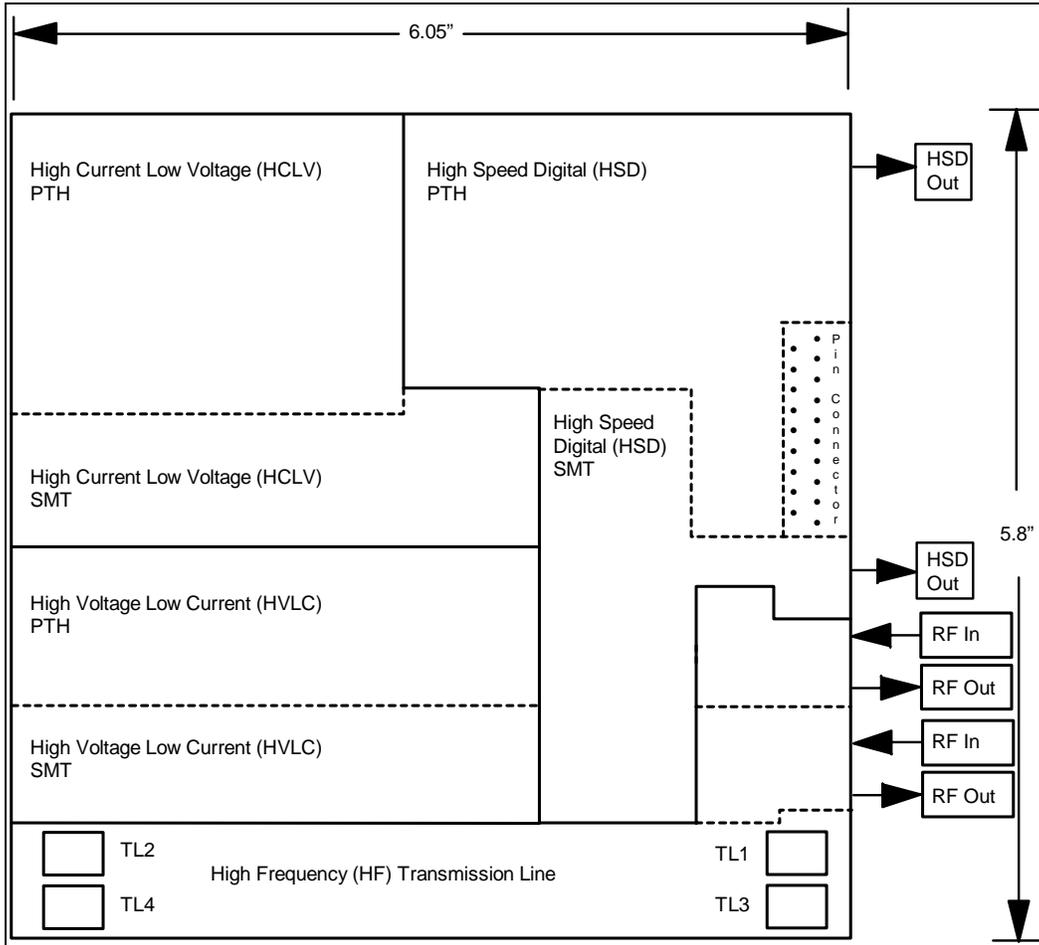


Figure 1. Layout of the PWA Illustrating the Major Sections and Subsections

2.2. Automated Test Set

The CCAMTF utilized an ATS to test the electrical performance of various sections of the PWA illustrated in Figure 1. The test set consists of a two-bay equipment cabinet, commercially available test equipment, a test fixture, computer, associated wiring, cable harnesses, and RF type coaxial cables. All commercial test equipment used is controlled by the general-purpose interface bus (GPIB, IEEE 488 standard). A further description of the ATS and the equipment and software incorporated therein can be found in Appendix C of the JTP.

2.3. Summary of Environmental Exposure Validation, Physical Reliability Validation, and Electrical Performance Tests.

The testing outlined in Tables 3 and Table 4 has been designed by the CCAMTF and is fully outlined in the JTP. Where applicable, testing of the multiple electrical sections found on the PWA was performed prior to, during, and upon completion of each validation testing sequence. A full description of these sections and the electrical tests performed on each can be found in Table 3 and Table 4, and Section 4.3 of this JTR.

Table 3. Environmental Exposure Validation Tests

Validation Test	JTP Section	Reference	Electrical Performance Test	JTP Section	Acceptance Criteria ^a
Environmental 85°C/85% Relative Humidity (RH)	3.4.1	IPC-TM-650, Method 2.6.3.3 MIL-PRF-38535D	HCLV	3.3.1	$\Delta V < 0.50 \text{ V}$
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	$\leq 20\%$ increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.6	$\geq 5 \times 10^7 \Omega$
			SW	3.3.7	$\Delta V < 0.356 \text{ V}$
Condensing Atmosphere	3.4.2	MIL-STD-883E, Method 1004.7	HCLV	3.3.1	$\Delta V < 0.50 \text{ V}$
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	$\leq 20\%$ increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.6	$\geq 5 \times 10^7 \Omega$
			SW	3.3.7	$\Delta V < 0.356 \text{ V}$
Fluid Exposure – Diesel Fuel	3.4.3	SAE J1211	HCLV	3.3.1	$\Delta V < 0.50 \text{ V}$
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	$\leq 20\%$ increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.6	$\geq 5 \times 10^7 \Omega$
			SW	3.3.7	$\Delta V < 0.356 \text{ V}$
Fluid Exposure - Hydraulic Fluid	3.4.4	SAE J1211	HCLV	3.3.1	$\Delta V < 0.50 \text{ V}$
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	$\leq 20\%$ increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.6	$\geq 5 \times 10^7 \Omega$
			SW	3.3.7	$\Delta V < 0.356 \text{ V}$

N/A = Not Applicable

HCLV = high current, low voltage

HVLC = high voltage, low current

HSD = high speed digital

HF = high frequency

ON = other networks

SW = stranded wire

^a Failure of a test board in a specific test does not necessarily disqualify a conformal coating process or alternative surface finish for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.

(Table 3 continued on the next page)

Table 3. Environmental Exposure Validation Tests

Validation Test	JTP Section	Reference	Electrical Performance Test	JTP Section	Acceptance Criteria ^a
Branch Water Test (Condensed Moisture Test)	3.4.5	N/A	HCLV	3.3.1	$\Delta V < 0.50 \text{ V}$
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	$\leq 20\%$ increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.6	$\geq 5 \times 10^7 \Omega$
			SW	3.3.7	$\Delta V < 0.356 \text{ V}$
Accelerated Life Test	3.4.6	N/A	HCLV	3.3.1	$\Delta V < 0.50 \text{ V}$
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	$\leq 20\%$ increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.6	$\geq 5 \times 10^7 \Omega$
			SW	3.3.7	$\Delta V < 0.356 \text{ V}$
Sulfur Dioxide/Salt Fog Resistance	3.4.7	N/A	HCLV	3.3.1	$\Delta V < 0.50 \text{ V}$
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	$\leq 20\%$ increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.6	$\geq 5 \times 10^7 \Omega$
			SW	3.3.7	$\Delta V < 0.356 \text{ V}$

N/A = Not Applicable

HCLV = high current, low voltage

HVLC = high voltage, low current

HSD = high speed digital

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ON = other networks

SW = stranded wire

^a Failure of a test board in a specific test does not necessarily disqualify a conformal coating process or alternative surface finish for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.

Table 4. Physical Reliability Validation Tests

Validation Test	JTP Section	Reference	Electrical Performance Test	JTP Section	Acceptance Criteria ^a
Thermal Shock	3.5.1	N/A	HCLV	3.3.1	$\Delta V < 0.50 \text{ V}$
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	$\leq 20\%$ increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.6	$\geq 5 \times 10^7 \Omega$
			SW	3.3.7	$\Delta V < 0.356 \text{ V}$
Thermal Cycling	3.5.2	N/A	HCLV	3.3.1	$\Delta V < 0.50 \text{ V}$
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	$\leq 20\%$ increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.6	$\geq 5 \times 10^7 \Omega$
			SW	3.3.7	$\Delta V < 0.356 \text{ V}$
Vibration	3.5.3	N/A	HCLV	3.3.1	$\Delta V < 0.50 \text{ V}$
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	$\leq 20\%$ increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.6	$\geq 5 \times 10^7 \Omega$
			SW	3.3.7	$\Delta V < 0.356 \text{ V}$
Mechanical Shock	3.5.4	N/A	HCLV	3.3.1	$\Delta V < 0.50 \text{ V}$
			HVLC	3.3.2	4 to 6 μA
			HSD	3.3.3	$\leq 20\%$ increase in propagation delay time from baseline
			HF	3.3.4	See JTP Tables 29 and 30
			ON	3.3.6	$\geq 5 \times 10^7 \Omega$
			SW	3.3.7	$\Delta V < 0.356 \text{ V}$

N/A = Not Applicable

HCLV = high current, low voltage

HVLC = high voltage, low current

HSD = high speed digital

HF = high frequency

ON = other networks

SW = stranded wire

^a Failure of a test board in a specific test does not necessarily disqualify a conformal coating process or alternative surface finish for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.

2.4. Validation Test Flow

The validation testing was performed in two sequential phases that were preceded with a screening phase. The validation phases and the testing performed therein were defined by the CCAMTF technical representatives. The testing sequences were designed to maximize the number of tests that were run on each set of PWAs. This testing sequence is outlined in Figure 2.

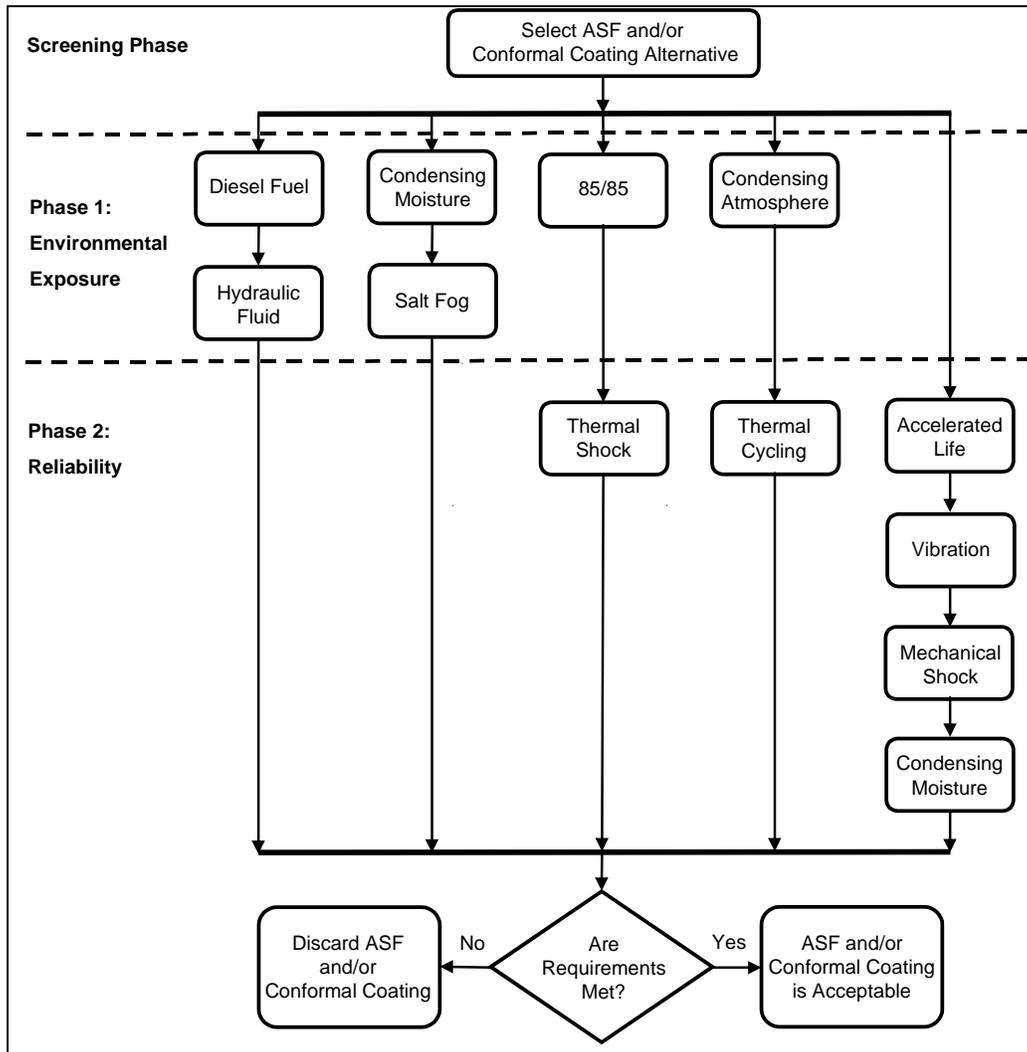


Figure 2. Sequences for the CCAMTF Validation Testing

2.5. Deviations from the JTP

Salt Fog (SF) Post Testing – Electrical retesting of anomalies following the SF test sequence was not conducted due to arcing of the PWAs, and the potential for damaging the testing equipment due to over ranging of the ammeter of the ATS.

Upon further discussion between the technical stakeholders regarding the electrical testing concerns experienced following the SF, a determination could not be made regarding the root cause of the arcing (PWAs) and over ranging (ATS) measurements. One potential explanation discussed was the heavily corroded PWA connectors due to a lack of masking. The JTP test protocol did not specify that the connectors should be masked prior to being placed in the SF chamber. Another potential cause for the high level of anomalies following the SF test could have been caused by corrosion sustained on most of the PWAs themselves.

Second Assembly Build (AL-Vib-MS-BW) - Due to the addition of the Accelerated life test sequence, a second PWA build sequence was required that introduced variation into the testing. These potential variation sources include:

- Change in PWA fabrication run
- Change in PWA assembly run, location, process/equipment.
- Parts Obsolescence – in particular, the 20 pin device was changed from a CLCC to a PLCC configuration.
- Parylene coating run, location and equipment.
- Silicone coating run and application spray software setup resulting in a change of coating quality, thickness & coverage between the two runs.

Urethane Coated PWAs – Included in the second build of LRSTF PWAs was the entire lot of urethane coated PWAs. Urethane was added to the test matrix after Phase I testing began. This second build of PWAs may have introduced an element of uncertainty due to nonrandomization of specimens during Phase I and Phase II testing. The exception being the AL-Vib-MS-BW test sequence, which was fully randomized. This is to say that if the urethane coated PWAs appear to have a significant effect on performance it may be caused by a change in materials, or changes due to new batches of components.

Branch Water (BW) Vertical Position Test, Extended Cable – A factor is required to be incorporated into the ATS software to account for the extra cable required to reach the test chamber from the HSD section of the PWA. This factor is required due the HSD test measuring the total propagation delay, and the sensitivity of this test to the cable length. It was found that following the BW vertical position test, a high number of anomalies were found for all coating/surface finish combinations. These anomalies were later attributed to an incorrect factor programmed into the ATS software. This factor was then corrected and the BW testing was completed as described in the Section 3.3.3 of the JTP. The results of the BW testing can be found in Appendix D following this report.

3.0 ALTERNATIVES TESTED

The CCAMTF initially conducted a screening program to select surface finishes and conformal coatings for evaluation. The details of this screening process and the results produced from the screening testing are documented in Iman, Koon, et al, (1997) “Screening Test Results for Developing Guidelines for Conformal Coating Usage and for Evaluating Alternative Surface Finishes,” CCAMTF Report, (June). Upon completion of the screening phase the following conformal coatings and alternative surface finishes (discussed in Section 3.1 and Section 3.2 of this JTR respectively) were chosen by the CCAMTF to be evaluated in the validation testing phases.

3.1 Conformal Coatings

3.1.1 Background

Conformal coating is widely applied to circuit cards to protect against adverse operating conditions. The application process is costly and time consuming. It is also the source of up to 40% of VOCs produced in some high-volume manufacturing operations and requires the use of pollution prevention equipment. Many manufacturers believe that conformal coating often adds unneeded cost to their processing that could be eliminated in specific applications without lowering quality or performance. A reduction in the use of conformal coatings without primers, would decrease manufacturing costs, simplify rework, and reduce pollution at the source.

3.1.2. Alternative Conformal Coatings

The following conformal coatings listed in Table 5 were chosen for evaluation during the environmental exposure and physical reliability testing phases.

Table 5. Conformal Coating Alternatives Tested During Validation Phase

Conformal Coating	Trade Name	Vendor	Processed
Urethane	Conathane CE 1175	Cytec	Raytheon, Ca.
Silicone	3-1753	Dow-Corning	Raytheon, Tx.
Parylene	Parylene C	Specialty Coating Systems	Raytheon, Ca.

The data obtained from the subsequent testing were then compared to that of uncoated PWAs. The results of this testing can be found in Section 6 and Appendices D through F of this JTR.

3.2. Surface Finishes

3.2.1. Background

Surface finishes are applied to PWAs to prevent oxidation of exposed copper conductors on the board, thus ensuring a solderable surface when components are added later. The most widely used processes are HASL with solder mask and reflowed tin-lead. In both processes, tin-lead is fused on exposed copper surfaces. In the HASL process, the PWA is fluxed and then dipped in liquid solder. As the PWA exits the solder dip, the excess solder is removed with hot air knives (hot air solder leveling). In the plated and reflowed SnPb process, SnPb is plated on the copper conductors and then reflowed by dipping in a hot oil bath. Besides being a source of lead waste in the environment, a major concern associated with these processes is their inability to provide a level-soldering surface. Planarity is extremely important in placing fine pitch components, which are becoming more prevalent in surface mount operations. The fused tin-lead surface finish is a limiting technology with respect to planarity. The aforementioned limitations led the CCAMTF to pursue alternative surface finishes.

3.2.2. Alternative Surface Finishes

The following alternative surface finishes listed in Table 6 were chosen based upon the screening test results.

Table 6. Alternative Surface Finishes Tested During Validation Phase

Surface Finish	Trade Name	Vendor	Processed
Benzimidazole	Entech 106A [©]	NA	RSC Austin, Tx.
Immersion Ag	AlphaLevel 3000 [©]	NA	Alpha Metals
Immersion Au/Pd	AuRo Tech [®]	NA	Lucent Technologies
HASL	Super HASL	NA	Lucent Technologies

NA – Not Available

These alternatives were then applied to the PWAs and Phase I and Phase II of the validation testing were conducted. The results obtained for the three alternatives were then compared to not only each other, but also that of HASL. These results can be found in Section 6 and Appendices D through F of this JTR.

4.0 TESTING BACKGROUND

All testing was performed in accordance with the JTP unless otherwise specified in Section 4.2.4 of the JTR. Section 4.3 and Section 4.4 respectively, contain overviews of the testing procedures performed in the environmental exposure and physical reliability sections of the JTP. Section 4.2 outlines the electrical performance tests that were run during each of the phases. These tests were run before, concurrently, and following the testing procedures that made up Phase I and Phase II of the validation testing. An outline of the screening tests run prior to the validation phase of this project can be found in Section 4.1 of this JTR and Section 3.1 and Section 3.2 of the JTP.

4.1 Screening Tests

Screening tests were first conducted on a number of different testing coupons to determine which alternate surface finishes and conformal coatings would be tested. The criteria used to evaluate these coupons and the tests that were performed for the initial screening tests can be found in Section 4.1.1 and Section 4.1.2 of this JTR. For complete descriptions of the testing coupons and the tests run during the screening phase please refer to Section 2.1, Section 3.1 and Section 3.2 of the JTP. Flow diagrams for the alternative surface finish and conformal coating screening tests can be found in the JTP labeled as Figure 5 and Figure 6 respectively in Section 2.6.

4.1.1 Alternative Surface Finish Screening Test Summary

The ASF screening tests were used to evaluate several critical properties of ASFs as put forth by the CCAMTF. These tests were used to reveal those finishes that would not meet the acceptance criteria set forth by the CCAMTF. This allowed non-conforming ASFs to be eliminated and allowed those which meet the requirements of the CCAMTF to be further tested during the evaluation phases as outlined in Sections 4.3 and 4.4 of this JTR.

Table 7 contains a listing of the screening tests performed for ASFs along with the applicable JTP section, acceptance criteria, and industrial reference. It should be noted that the test description, rationale, methodology, any major or unique equipment required, and any data recording and calculations required can be found in the appropriately noted JTP sections.

Table 7. Alternative Surface Finish Screening Tests

Screening Test	JTP Section	Reference	Acceptance Criteria
Surface Insulation Resistance (SIR)	3.1.1	IPC-TM-650, Method 2.6.3.3	$\geq 10^8 \Omega$
Electromigration	3.1.2	IPC-TM-650, Method 2.6.14	$\geq 10^5 \Omega$
Solderability	3.1.3	ANSI/J-STD-003	Solder wetting force at 2 seconds \geq hot-air solder leveling (HASL) baseline surface finish performance
Contamination Characterization (Extended Test) ^a	3.1.4	IPC-TM-650, Method 2.3.28	Low-residue flux finished assemblies: (expected contamination) $Cl^- < 2.5 \mu g/in^2$ $Br^- < 15 \mu g/in^2$ Water-soluble flux finished assemblies: (expected contamination) $Cl^- < 4.5 \mu g/in^2$ $Br^- < 15 \mu g/in^2$

^a The contamination characterization test is not required by all defense system programs, and is therefore known as an “extended test.” The test may be performed at the discretion of each specific defense system program.

4.1.2 Conformal Coating Screening Test Summary

The conformal coating screening tests were initial tests used to evaluate several critical properties of conformal coatings. Table 8 contains a summary of the conformal coating screening tests. It should be noted that as with the ASF screening tests the test description, rationale, methodology, any major or unique equipment required, and any data recording and calculations required can be found in the appropriately noted JTP sections.

Table 8. Conformal Coating Screening Tests

Screening Test	JTP Section	Reference	Supporting Test	JTP Section	Acceptance Criteria
Coating Thickness	3.2.1	ASTM D 1005-95	N/A	N/A	<ul style="list-style-type: none"> Acrylic resin, epoxy resin, and urethane resin: 0.002 ± 0.001 inch Silicone resin: 0.005 ± 0.003 inch Parylene: 0.0005 to 0.0020 inch
Fungus Resistance	3.2.2	ASTM G 21-90	N/A	N/A	<ul style="list-style-type: none"> Rating of 0
Flexibility	3.2.3	FED-STD-141C, Method 6221	N/A	N/A	<ul style="list-style-type: none"> No cracking or crazing
Flame Resistance	3.2.4	ASTM D 635-91	N/A	N/A	<ul style="list-style-type: none"> Self-extinguishing or non-burning
Resonance	3.2.5	MIL-I-46058C	N/A	N/A	<ul style="list-style-type: none"> The minimum Q value for uncoated type GF laminates at frequencies of 1 and 50 MHz shall be 50 and 70, respectively.^a
Thermal Shock	3.2.6	MIL-STD-202, Method 107G	Dielectric Withstanding Voltage	3.2.7	<ul style="list-style-type: none"> ≤ 10 μA
Dielectric Withstanding Voltage	3.2.7	MIL-STD-202F, Method 301	N/A	N/A	<ul style="list-style-type: none"> ≤ 10 μA

N/A = Not Applicable

(Table 8 continued on next page)

^a See Section 3.2.7 of the JTP for the maximum allowable changes due to the application of coatings.

^b The supporting adhesion test can be referenced in ASTM D 3359-95a.

Table 8. Conformal Coating Screening Tests (Continued)

Screening Test	JTP Section	Reference	Supporting Test	JTP Section	Acceptance Criteria
Insulation Resistance	3.2.8	MIL-STD-202, Method 302	N/A	N/A	<ul style="list-style-type: none"> • Each specimen $\geq 1.5 \times 10^{12} \Omega$ • Average specimen $\geq 2.5 \times 10^{12} \Omega$
Moisture Resistance	3.2.9	MIL-STD-202, Method 106	Dielectric Withstanding Voltage	3.2.7	<ul style="list-style-type: none"> • $\leq 10 \mu\text{A}$
			Insulation Resistance	3.2.8	<ul style="list-style-type: none"> • Each acrylic resin, silicone resin, urethane resin, parylene $\geq 5.0 \times 10^9 \Omega$ • Each epoxy resin $\geq 5.0 \times 10^8 \Omega$ • Average acrylic resin, silicone resin, urethane resin, parylene $\geq 1.0 \times 10^{10} \Omega$ • Average epoxy resin $\geq 1.0 \times 10^9 \Omega$
Thermal Humidity Aging	3.2.10	MIL-I-46058C	N/A	N/A	<ul style="list-style-type: none"> • No evidence of reversion • No loss of legibility
			Adhesion ^b	3.2.11	<ul style="list-style-type: none"> • Rating ≥ 4
Adhesion	3.2.11	ASTM D 3359-95a	N/A	N/A	<ul style="list-style-type: none"> • Rating ≥ 4

N/A = Not Applicable

^a See Section 3.2.7 of the JTP for the maximum allowable changes due to the application of coatings.

^b The supporting adhesion test can be referenced in ASTM D 3359-95a.

4.2 PWA Testing Matrix

Section 4.3 contains the descriptions and rationale for the electrical performance tests that were conducted during the environmental and physical reliability phases of the testing. Section 4.4 and Section 4.5 contain descriptions of the environmental exposure and physical reliability tests that were conducted during Phase I and Phase 2 of the CCAMTF testing sequences. Prior to performing these tests the PWAs were coated with the alternative conformal coatings, and alternative surface finishes discussed in Section 3.1 and Section 3.2 along with either the WS or LR solder.

The PWAs were then divided into four groups with each group receiving one of the four surface finishes (HASL, Benzimidazole, Immersion Silver (Ag), or Immersion Gold/Palladium (Au/Pd)). These four groups of PWAs were then further divided into two groups each. These groups received either LR or WS solder. These eight groups were then further divided into four sub-groups. These groups were then coated with one of the three potential conformal coatings with one group receiving no coating. A total of five PWAs were produced for each surface finish/flux/conformal coating combination (four surface finishes X 4 conformal coatings X 2 flux types X 5 PWAs per combination) giving a total of 160 PWAs for each testing sequence described in Figure 1. For each PWA 23 individual electrical circuits were tested (23 circuits X 160 PWAs) yielding 3680 data points. These 23 electrical circuits are outlined in Table 9.

Table 9. Electrical Responses for the LRSTF PWA

Response	Circuitry	JTP Acceptance Criteria
High Current Low Voltage		
1	HCLV PTH	Δ Voltage from Pre-test < 0.50V
2	HCLV SMT	Δ Voltage from Pre-test < 0.50V
High Voltage Low Current		
3	HVLC PTH	$4\mu\text{A} < X < 6\mu\text{A}$
4	HVLC SMT	$4\mu\text{A} < X < 6\mu\text{A}$
High Speed Digital		
5	HSD PTH Propagation Delay	< 20% increase from Pre-test
6	HSD SMT Propagation Delay	< 20% increase from Pre-test
High Frequency Low Pass Filter		
7	HF PTH 50 MHz	$\pm 5\text{dB}$ of HASL LR Parylene average
8	HF PTH f(-3dB)	$\pm 50\text{MHz}$ of HASL LR Parylene average
9	HF PTH f(-40dB)	$\pm 50\text{MHz}$ of HASL LR Parylene average
10	HF SMT 50 MHz	$\pm 5\text{dB}$ of HASL LR Parylene average
11	HF SMT f(-3dB)	$\pm 50\text{MHz}$ of HASL LR Parylene average
12	HF SMT f(-40dB)	$\pm 50\text{MHz}$ of HASL LR Parylene average

(Table 9 continued on next page)

Table 9 Electrical Responses for the LRSTF PWA (continued)

Response	Circuitry	JTP Acceptance Criteria
High Frequency Transmission Line Coupler		
13	HF TLC 50MHz Forward Response	±5dB of Pre-test
14	HF TLC 500MHz Forward Response	±5dB of Pre-test
15	HF TLC 1GHz Forward Response	±5dB of Pre-test
16	HF TLC Reverse Null Frequency	±50MHz of Pre-test
17	HF TLC Reverse Null Response	< 10dB increase over Pre-test
Other Networks—Leakage		
18	10 mil Pads	Resistance > 7.7 log ₁₀ ohms
19	PGA A	Resistance > 7.7 log ₁₀ ohms
20	PGA B	Resistance > 7.7 log ₁₀ ohms
21	Gull Wing	Resistance > 7.7 log ₁₀ ohms
Stranded Wire		
22	Stranded Wire 1	Δ Voltage from Pre-test < 0.356V
23	Stranded Wire 2	Δ Voltage from Pre-test < 0.356V

4.3. Electrical Performance Tests

Sections 4.3.1 through 4.3.7 contain basic descriptions and the rationale for the electrical performance tests that were conducted prior to, during, and following the environmental exposure and physical reliability test sequences described in Section 4.4 and Section 4.5 respectively. Unless otherwise specified electrical performance tests were performed on each PWA prior to, during and following all applicable validation tests. For a more detailed description of these tests including methodology, major or unique equipment, data recording and calculations, parameters, and acceptance) please refer to the JTP Section 3.3. Acceptance criteria can also found in Table 3 of this JTR

4.3.1 High Current, Low Voltage

4.3.1.1 Description

This test determines the resistance in a circuit as a function of voltage.

4.3.1.2 Rationale

Performance of high-current circuits is affected by series resistance. Resistance is most likely to change due to cracking or corrosion of the solder joint that may be related to the soldering process. These conditions decrease the cross-sectional area of the solder joints, thus increasing resistance. Use of high current to test solder-joint resistance makes it easier to detect a change in resistance. A 5 A Amperes (A) current has been selected as a

value that covers most military applications. A change of resistance is most conveniently determined by measuring the steady state performance of the circuit at a pulse width of 100 μ s. This pulse width is long enough for the circuit to achieve steady state before the measurement is taken.

4.3.2 High Voltage, Low Current

4.3.2.1 Description

This test determines changes in resistance as a function of current when a high voltage is applied to a circuit.

4.3.2.2 Rationale

The insulation resistance between conductors may be reduced by flux residues, surface finish, and conformal coating. The impact of this decrease in resistance could be significant in circuits with a high-voltage gradient across the insulating region. Decreased resistance can be detected by an increase in current when a high voltage is applied to the circuit. A voltage of 250V was selected as the high potential for this test because it represents most military applications. The change in leakage current is determined by measuring the steady-state output of the circuit.

4.3.3 High Speed Digital

4.3.3.1 Description

HSD testing will be used to determine the gate switching speed of an integrated circuit.

4.3.3.2 Rationale

The gate switching speed will be affected by the presence of flux residues, surface finish, conformal coating and environmental conditions.

4.3.4 High Frequency, Low Pass Filter

4.3.4.1 Description

This test determines surface finish and conformal coating film effects on the performance of high-frequency, LPF printed circuit inductors and transmission lines caused by parasitic resistance and parasitic capacitance.

4.3.4.2 Rationale

Changes in surface finish, conformal coating, or flux residues may affect the performance of LPF printed circuit inductors and transmission lines due to parasitic resistance and parasitic capacitance. When a sine wave test signal is passed through an LPF, its amplitude is attenuated as a function of frequency. The relationship between the output and input voltage amplitudes can be expressed as a transfer function. The transfer function, V_{out} / V_{in} , can be measured to determine effects of changes in surface finish, conformal coating, or flux residues.

4.3.5 High-Frequency Transmission Line Coupler

4.3.5.1 Description

This test determines surface finish and conformal coating film effects on the performance of high frequency Transmission Line Couplers (TLCs) caused by parasitic resistance and parasitic capacitance.

4.3.5.2 Rationale

Surface finish, conformal coating, or flux residues may affect the performance of LPF printed circuit inductors and transmission lines due to parasitic resistance and parasitic capacitance.

4.3.6 Other Networks

4.3.6.1 Description

This test determines the current leakage for a typical circuit layout as a function of processing, surface finishing, conformal coating, and environmental conditions. Leakage current will be expressed as a function of surface insulation resistance.

4.3.6.2 Rationale

The pin-grid array, gull wing, and 10-mil pads (see Appendix B) allow leakage currents to be measured. The presence of residues combined with the environmental exposure may increase current leakage.

4.3.7 Stranded Wires

4.3.7.1 Description

This test determines the resistance in an insulated 22-gauge stranded wire circuit as a function of voltage.

4.3.7.2 Rationale

Performance of high-current circuits is affected by series resistance. Resistance is most likely to change due to cracking or corrosion of the conductor that may be related to the soldering process. These conditions decrease the cross-sectional area of the solder joints, thus increasing resistance. Use of high current to test solder joint resistance makes it easier to detect a change in resistance. A 5 A current has been selected as a value that covers most military applications. A change of resistance is most conveniently determined by measuring the steady state performance of the circuit at a pulse width of 100 μ s. This pulse width is long enough for the circuit to achieve a steady state before the measurement is taken.

4.4 Environmental Exposure Testing

Sections 4.4.1 through 4.4.4 offer descriptions and rationale for the environmental exposure validation testing. Physical reliability testing descriptions and rationale can be found in Section 4.5.1 through Section 4.5.4. For more thorough and in-depth test summaries, including test procedure, methodology, major equipment or unique equipment required, and data recording and calculations performed please refer to the JTP Section 3.4. Results for these tests can be found in Section 6 of the JTR.

4.4.1 85°C/85% Relative Humidity

4.4.1.1 Purpose

This test determines a test specimen's performance after exposure to thermal-humidity aging conditions.

4.4.1.2 Rationale

MIL-PRF-38535D (*General Specification for Integrated Circuits (Microcircuits) Manufacturing*, April 15, 1996) specifies this test to evaluate circuits. IPC-TM-650 Method 2.6.3.3 Rev. A (*Surface Insulation Resistance, Fluxes*, January 1995) also specifies this test.

4.4.2 Condensing Atmosphere

4.4.2.1 Purpose

This evaluation determines a specimen's performance under condensing moisture conditions.

4.4.2.2 Rationale

MIL-STD-883E Method 1004.7 (*Test Method Standard Microcircuits, Moisture Resistance*, August 17, 1987) specifies this test to evaluate moisture resistance.

4.4.3 Fluid Exposure-Diesel Fuel

4.4.3.1 Purpose

This test determines a test specimen's resistance to degradation from contact with diesel fuel.

4.4.3.2 Rationale

This test is based on the requirements of SAE J1211 (*Recommended Environmental Practices for Electronic Equipment Design*, November 1978). Diesel fuel is a typical fluid encountered in military applications.

4.4.4 Fluid Exposure-Hydraulic Fluid

4.4.4.1 Purpose

This evaluation determines a specimen's resistance to degradation from contact with hydraulic fluid.

4.4.4.2 Rationale

This test is based on the requirements of SAE J1211 (*Recommended Environmental Practices for Electronic Equipment Design*, November 1978). Hydraulic fluid is a typical fluid encountered in military applications.

4.4.5 Branch Water Test (Condensed Moisture Test)

4.4.5.1 Purpose

This test determines the moisture condensation protection provided by a conformal coating film.

4.4.5.2 Rationale

This test is based on the requirements of MIL-E-5400T (*General Specification for Aerospace Electronic Equipment*, August 14, 1992) and MIL-STD-810. The surfactant is added as a small percentage by volume to lower the surface tension of the solution and achieve a continuous aqueous film across the entire surface of the PWA.

4.4.6 Accelerated Life Test

4.4.6.1 Purpose

This test determines the long-term performance of a solder joint connection.

4.4.6.2 Rationale

This test is based on identified needs of the defense system programs. The background of this test was taken from Engelmaier's paper (*The Use Environments of Electronic Assemblies and Their Impact on Surface Mount Solder Attachment Reliability*, January 1990).

4.4.7 Sulfur Dioxide/Salt Fog Resistance

4.4.7.1 Purpose

This test determines the resistance of a conformal coating film to accelerated, deleterious effects of exposure to a sulfur dioxide/salt fog.

4.4.7.2 Rationale

This test simulates the environmental conditions typically experienced by a defense system situated on an aircraft carrier or on shore locations with considerable air pollution.

4.5 Physical Reliability Evaluation

The following sections outline the physical reliability testing sequences performed during Phase II testing. For more thorough and in-depth test summaries, including test procedure, methodology, major equipment or unique equipment required, and data recording and calculations performed please refer to the Section 3.5 of the JTP. Results for the physical reliability testing described in the following sections can be found in Section 6 of this JTR.

4.5.1 Thermal Shock

4.5.1.1 Purpose

This evaluation determines the effect of instantaneous changes between low and high temperature on a specimen.

4.5.1.2 Rationale

This evaluation is based on the requirements of MIL-STD-883E, Method 1010.7 Condition B (*Test Method Standard Microcircuits, Temperature Cycling*, May 1987).

4.5.2 Thermal Cycling

4.5.2.1 Purpose

This evaluation determines the effect of thermal stresses due to a coefficient of thermal expansion (CTE) mismatch on the electrical performance of a PWA.

4.5.2.2 Rationale

This evaluation is based on the requirements of MIL-STD-781D (*Reliability Testing for Engineering Development, Qualification, and Production*, October 1986). Thermal cycling evaluations are commonly used for environmental stress screening for infant mortality and qualification testing of PWAs.

4.5.3 Vibration

4.5.3.1 Purpose

This evaluation determines the effect of vibration on a specimen.

4.5.3.2 Rationale

This evaluation is based on the requirements of MIL-STD-810E, Method 514.4 (*Test Method Standard for Environmental Engineering Consideration and Laboratory Tests, Vibrational*, July 1989). Vibration testing is performed to determine the equipment resistance to vibrational stresses expected during its shipment and use. Vibration can cause wire chafing, loosening of fasteners, intermittent electrical contacts, touching and shorting of electrical parts, seal deformation, component fatigue, optical misalignment, cracking, and rupturing.

4.5.4 Mechanical Shock

4.5.4.1 Purpose

This evaluation determines a specimen's resistance to impact.

4.5.4.2 Rationale

This evaluation is based on the requirements of MIL-STD-810E Method 516.4. (*Test Method Standard for Environmental Engineering Consideration and Laboratory Tests, Shock*, July 1989). Mechanical shock evaluations are commonly used to ensure solder joint strength. This test will determine whether the PWA has maintained sufficient solder joint strength.

5.0 VALIDATION TESTING RESULTS

In the following sections, the results for the validation testing sequences will be presented. These results are given for each environmental exposure sequence, and also each physical reliability sequence. These sequences are further broken down to show results for individual tests (i.e., diesel fuel exposure, hydraulic fluid...). For each test all of the previously described electrical responses were recorded before, during and after testing were applicable. Table 10 provides a summary of the yields (percentage meeting the JTP acceptance criteria) for each test environment.

Complete testing results for all environmental and physical reliability tests conducted showing individual surface finish, conformal coating, and flux performance can be found in Appendices D through F. The reader will find, in these appendices, detailed test protocols for all testing performed along with in-depth statistical analysis for all electrical responses measured.

Table 10. Summary of Yields (Percentage) By Circuit Group For Each Environmental Test

Diesel Fuel-Hydraulic Fluid Exposure								
	HCLV	HVLC	HSD	HF LPF	HF TLC	ON	SW	TOTALS
DF	99.1	98.1	100.0	99.2	99.4	100.0	100.0	99.4
HF	100.0	100.0	100.0	98.2	99.3	100.0	100.0	99.6
Averages	99.6	99.1	100.0	98.7	99.4	100.0	100.0	99.5
Branch Water-Salt Fog								
BW Vertical	98.4	10.3	6.9	98.9	49.8	34.8	100.0	61.4
BW Post Vertical	99.7	97.5	99.7	99.6	97.5	99.5	100.0	99.0
BW Horz Backside	99.7	38.1	78.1	93.3	40.5	49.4	100.0	69.2
BW Post Backside	99.7	97.8	100.0	99.2	97.4	99.4	100.0	98.9
BW Horz Comp Up	99.1	6.9	83.1	99.2	90.3	34.5	100.0	76.6
BW Post Comp	99.7	98.4	100.0	99.7	97.6	96.6	100.0	98.6
Salt Fog	84.7	9.7	48.1	68.2	72.3	39.4	95.0	61.0
Averages	99.4	58.2	78.0	98.3	78.9	69.0	100.0	84.0
85/85-Thermal Shock								
85/85	99.7	96.9	100.0	99.4	99.5	98.1	100.0	99.1
Thermal Shock	99.7	96.9	100.0	98.8	99.4	99.4	100.0	99.1
Averages	99.7	96.9	100.0	99.1	99.5	98.8	100.0	99.1
Condensing Atmosphere-Thermal Cycle								
CA Cycle 10	100.0	58.8	98.4	99.7	93.5	64.1	100.0	88.5
Thermal Cycle	99.1	99.4	100.0	99.5	98.3	99.1	99.4	99.2
Averages	99.6	79.1	99.2	99.6	95.9	81.6	99.7	93.9

Note: Shaded entries designate low yields

(Table 10 continued on next page)

Table 10. Summary Of Yields (Percentage) By Circuit Group For Each Environmental Test (continued)

Accelerated Life-Vibration-Mechanical Shock-Branch Water								
	HCLV	HVLC	HSD	HF LPF	HF TLC	ON	SW	TOTALS
Accelerated Life	100.0	99.7	100.0	99.7	97.5	100.0	100.0	99.3
Vibration	99.1	99.7	99.7	99.7	95.1	100.0	100.0	98.7
Mechanical Shock	99.4	95.6	99.7	99.3	97.5	99.7	100.0	98.8
BW Vertical	99.1	15.0	11.9	98.6	88.6	49.7	100.0	73.3
BW Post Vertical	99.1	90.9	99.7	99.4	95.1	97.2	100.0	97.4
Averages	99.3	80.2	82.2	99.3	94.8	89.3	100.0	93.5

Note: Shaded entries designate low yields

5.1 Environmental Exposure

5.1.1 Summary of Results for Exposure to Diesel Fuel and Hydraulic Fluid

Following Pre-test, 160 PWAs were twice dipped in diesel fuel (DF) for 10 minutes (min), dried, and retested. Next, they were twice dipped in hydraulic fluid (HF) for 10 min, dried, and retested. As is true of all test environments, 3680 electrical measurements were recorded at each test time and compared to the JTP acceptance criterion (see Table 3 in Section 2.3). Sixteen of the 23 circuits on the LRSTF PWA survived exposure to DF and HF with no anomalies while the remaining seven circuits had only 14 anomalies. Table 10 provides a summary of the yields (percentage meeting the JTP acceptance criteria) for each test environment. This table shows that the yields were quite high (98.2% to 100%) for all circuits throughout the DF-HF test sequence.

Only two test measurements were of sufficient magnitude relative to the JTP acceptance criteria to be considered for failure analysis. In addition to these anomalies, there were 13 HSD circuits that did not respond. Failure analysis revealed that the damage sustained in the HSD section was due to electrical overstress (EOS), which damaged either the active components or the circuit traces. The source of the EOS was likely from the adjacent ON (leakage current) section of the PWA, which was biased with 100V.

Statistical analysis showed no relationship between the number of anomalies and surface finish in the DF-HF test sequence. Conformal coating was not beneficial relative to the JTP acceptance criteria taken over all 23 circuits. This is not to say that coating would not be beneficial to some circuits in some instances, but rather coating was not an important factor in determining the number of anomalies that did not meet the JTP acceptance criteria in the DF-HF test sequence. Likewise, flux type was not an important factor relative to the number of anomalies.

5.1.2 Summary of Test Results for Exposure to Branch Water and Salt Fog

Following pre-test, a second set of 160 PWAs were sprayed with a detergent solution and tested while wet and again after drying. In the first part of the BW test, both sides of a PWA were sprayed while it was in a vertical position. After testing, the PWA was placed in a horizontal position with the backside up and only the uppermost side was sprayed. This test was repeated with the component side up. Following the BW test, the PWAs were exposed to an extremely harsh environment consisting of 83 cycles in a salt fog chamber, which took 500 hr to complete.

There were 1420 anomalies during the BW test performed in the vertical position. As shown in Table 10, the BW anomalies were mainly associated with HVLC, HSD, HF TLC, and ON circuits. Uncoated PWAs had significantly more anomalies than coated PWAs. On the other hand, the anomalies were uniformly spread over surface finishes and flux types. Table 9 shows the yield in the vertical position was only 61.4%. Following the vertical position test there were only 37 anomalies (yield = $3643/3680 = 99.0\%$).

There were 1134 anomalies during the horizontal position with the backside up. The reduction in the number of anomalies was due to correcting a software problem involving the correct cable length factor in the CCAMTF ATS for total propagation delay with HSD circuits. There were 780 ($780/1134 = 68.8\%$) carry over anomalies from the BW vertical position test. The median number of anomalies was 7 and the average number of anomalies per PWA is as follows for each coating state: uncoated (9.9), parylene (4.8), silicone (7.9), and urethane (5.9). Uncoated PWAs again had significantly more anomalies than coated PWAs while the anomalies were again uniformly spread over surface finishes and flux types. Table 10 shows the yield in the horizontal position (backside up) was 69.2%. Following the horizontal position there were only 41 anomalies (yield = 98.9%).

There were 860 anomalies during the horizontal position with the component side up. This is a reduction of 560 from the vertical position and 274 less than in the horizontal position with the backside up. This latest reduction was due to the HF TLC circuit, which utilizes transmission lines on the backside of the PWA, which do not get sprayed in this position. There were 546 carry over anomalies from the vertical and horizontal (backside up) positions. Every PWA had at least two anomalies and the median number of anomalies was 5. The average number of anomalies per PWA is as follows for each coating state: uncoated (6.9), parylene (5.7), silicone (4.3), and urethane (4.5). Both uncoated and parylene coated PWAs had significantly more anomalies than either silicone or urethane coated PWAs while the anomalies were again uniformly spread over surface finishes and flux types. Table 9 shows the yield in the horizontal position (component side up) was 76.6%. Following the BW horizontal position there were 50 anomalies (yield = $3630/3680 = 98.6\%$).

Following the BW test, the LRSTF PWAs were subjected to a SF test to determine the resistance of a conformal coating film to accelerated, deleterious effects of exposure to a

sulfur dioxide/salt fog. The PWAs were tested after 500 hr of SF exposure. Testing was quite difficult as the connectors were corroded, the uncoated boards arced during the HVLC and current leakage testing, and the HF tests showed abnormal waveforms. In addition, the ammeter over ranged or could not stabilize during many of the tests, which created unstable readings. Due to these concerns, anomalous measurements were not retested after SF as they were in all other stages of the CCAMTF test program. The SF test clearly presents an extremely harsh environment and not surprisingly, there were a large number (1435) of anomalies. In fact, every PWA had at least two anomalies and the median number of anomalies was nine.

The average numbers of anomalies per PWA for surface finishes after SF are: HASL (8.5), benzimidazole (9.2), immersion Ag (9.3), and immersion Au/Pd (8.9). The mean number of anomalies does not differ significantly for surface finishes. However, uncoated PWAs with an average of 11.2 anomalies per PWA had significantly more anomalies than coated PWAs. Urethane, with an average of 9.3, had significantly more anomalies than silicone with an average of 7.1, but was not significantly more than parylene with an average of 8.3. PWAs processed with either LR or WS flux each had an average of nine anomalies per PWA.

5.1.3 Summary of Test Results for Exposure to 85°C/85%RH and Thermal Shock

Following pre-test, a third set of 160 PWAs was subjected to a test sequence consisting of three weeks exposure in an environmental chamber with the temperature and relative humidity set to 85°C at 85%, respectively. This test was followed by a thermal shock (TS) test where all PWAs were mechanically rotated between chambers set at -50°C ± 5°C and 125°C ± 5°C. The TS test lasted for 200 cycles each cycle taking approximately 1 hr.

Table 10 shows that yields were quite high (96.9% to 100%) for all circuits throughout the 85/85-TS test sequence. The overall yield was 99.1% following both tests. The yields for surface finishes ranged from 98.6% (immersion Ag) to 99.6% (benzimidazole) at Post 85/85 and from 98.5% (immersion Ag) to 99.7% (benzimidazole) at 200TS. The corresponding ranges for coating categories were 98.6% (silicone) to 99.6% (parylene) at post 85/85 and 98.7% (uncoated) to 99.3% (silicone) following 200TS. Perhaps the most surprising result was how well uncoated PWAs fared. This group was slightly better than silicone coated PWAs at Post 85/85 and was only 0.7% behind the best performance recorded by parylene. Uncoated PWAs have the lowest yield at 200TS, but again are only 0.6% behind the best performance recorded by silicone.

At the conclusion of the 85/85 test, there were 33 anomalous measurements that did not meet the JTP acceptance criteria. Twenty of these anomalies carried over to 200TS. There were 14 new anomalies at TS200, bringing the total to 34 at the conclusion of the 85/85-TS test sequence. These 34 anomalies occurred on 24 PWAs. Of the 34 anomalies at 200TS, 21 were severe enough to be candidates for failure analysis. These 21 anomalies occurred on 16 PWAs with eight of the 21 anomalies occurring on just three

PWAs. The 16 PWAs with severe anomalies included all surface finishes, coating status, and flux.

In addition to these anomalies, there were 27 HSD circuits that did not respond after 200TS. These failures are typically attributable to damage sustained in the HSD section as previously explained. The 27 damaged HSD circuits occurred on 18 PWAs and were spread over all surface finishes, coating conditions, and flux types.

5.1.4 Summary of Test Results for Exposure to Condensing Atmosphere and Thermal Cycling

Following Pre-test, a fourth set of 160 PWAs was subjected to a test sequence consisting of 10 cycles in a condensing atmosphere (CA) chamber. This test was followed by a thermal cycle (TC) test where the temperature cycled between -55°C and 100°C . The TS test lasted for 500 cycles with each cycle having taking approximately 122 min.

The circuit yields in Table 10 range from 58.8% to 100% during Cycle 10. The HVLC (58.8%) and ON (64.1%) circuits had the lowest yields during Cycle 10 while all other circuits had yields of at least 93.5%. The overall yield during Cycle 10 was 88.5%. At 500 TC the yields ranged from 98.3% to 100% with an overall yield of 99.2%.

The yields for surface finishes ranged from 87.1% (HASL) to 90.4% (benzimidazole) during Cycle 10 and from 98.6% (immersion Ag) to 99.7% (benzimidazole) at 500TC. The yields for coating categories during Cycle 10 were uncoated (75.5%), urethane (87.3%), parylene (95.0%), and silicone (96.3%). At 500TC, the coating yields were very close with a range of 98.9% for silicone to 99.3% for both uncoated and parylene.

There were 422 anomalies that did not meet the JTP acceptance criteria during Cycle 10. The number of anomalies was reduced to only 30 at 500TC. Most of the decrease at 500TC was due to improvements in the performance of the HVLC and ON circuits. Statistical analyses showed no relationship between the number of anomalies and surface finish either during Cycle 10 or at 500TC. However, there was a strong relationship between the number of anomalies and coating status during Cycle 10 with uncoated and urethane coated PWAs having significantly more anomalies than either parylene or silicone. This relationship did not hold at 500TC. In addition to these 30 anomalies, there were nine HSD circuits that did not respond after 500TC. These failures are typically attributable to damage sustained in the HSD section as previously explained.

5.1.5 Summary of Test Results for Accelerated Life, Vibration, Mechanical Shock, and Branch Water

Following Pre-test, a fifth set of 160 PWAs was subjected to a test sequence consisting of accelerated life (AL) test, vibration (Vib), and mechanical shock (MS). The purpose of these tests was to determine if these environments would compromise the integrity of the

conformal coating. Following this test sequence, the PWAs were subjected to the worst case of the branch water (BW) test (i.e., PWAs in a vertical position).

Table 10 shows that all but four cases had yields of at least 99.1% during the AL-Vib-MS test sequence. The lowest yield during this sequence was 95.1%. On the other hand, the BW vertical position had a very adverse affect on HVLC, HSD, and ON. There were no differences in yields due to surface finishes during the BW vertical position as these yields ranged only from 92.6% (immersion Ag) to 93.7% (immersion Au/Pd). The yields for coating status were also quite close during this test time with a range of 92.4% (uncoated) to 94.9% (parylene).

There were 96 anomalies that did not meet the JTP acceptance criteria at the conclusion of the AL-Vib-MS-BW test sequence, which occurred on 67 PWAs. There was no significant difference due to either surface finish or flux type, but there was a strong significant difference due to coating status, with the uncoated PWAs having significantly more anomalies and parylene having significantly fewer. In addition to these 96 anomalies, there were 13 HSD PTH and 32 HSD SMT circuits that did not respond at Post BW. HSD PTH anomalies were always accompanied by a HSD SMT anomaly.

5.2 Adhesion Testing

The following sections contain brief discussions of the testing and results obtained regarding adhesive properties of conformal coatings with respect to the environmental and reliability tests that have been previously discussed. Refer to Appendix E for complete test results and data analysis, as provided by Raytheon Electronic Systems El Segundo, California.

5.2.1 Conformal Coatings Adhesion

Adhesion of conformal coatings is generally considered one of the most significant properties in evaluating a coating's performance, reliability and durability for a given application. Coating adhesion depends on processing conditions, the substrate to which it is applied and the end-use environment. Examples of assembly processing parameters affecting adhesion include; flux, solder, PWA material, PWA solder mask, soldering process, and PWA surface finish. Examples of end-use environments include temperature and humidity extremes, sand, salt-water, gases, petroleum based fluids, etc.

Adhesion of a conformal coating is the "strength" of the coating interaction with the surface to which it is applied. There are different methods for assessing adhesion ranging from qualitative observations to quantitative data analysis. Qualitative methods involve optical inspection at 10X magnification or "implied test methods" such as rub testing or wear testing. Quantitative or "direct" adhesion test methods result in generating some form of numerical data that can be considered as "measuring" adhesion.

One test method that utilizes both quantitative and qualitative measurement techniques is ASTM D 3359 entitled “Standard Test Methods for Measuring Adhesion by Tape Test”. The tape/peel test involves applying a pressure-sensitive adhesive (PSA) tape to the coated film and recording the resistance to and degree of film removed when the tape is removed. Since an intact film with appreciable adhesion is frequently not removed at all, the severity of the test is usually enhanced by cutting into the film a figure “X” or a cross-hatched lattice pattern by either successive single scribe cuts or by a single stroke with a multi-bladed tool or knife, before applying and removing the tape. The tape is rubbed over the scribed lattice area and then rapidly peeled. The adhesion is then assigned an integer rating when comparing the film removed against an established rating scale from 0 to 5 based on the following scale:

<u>Interpretation</u>	<u>Rating</u>
No noticeable removal of the coating	5
Less than 5% of the coating removed	4
5%-15% of the coating removed	3
15% - 35% of the coating removed	2
35% - 65% of the coating removed	1
More than 65% of the coating removed	0

If the tape peels the film cleanly, or if it debonds just by cutting into it without applying tape, then the adhesion is rated simply as poor or very poor. The physics of the tape being peeled as it relates to the coating stresses in peeling and the forces involved to overcome the coating’s physical bond to the applied substrate are detailed in numerous technical journals as well as the rationale of the ASTM specification. Details on the ASTM specification are summarized in Appendix E.

5.2.2 Adhesion Testing Conditions

Adhesion was measured on test vehicles assembled with two different fluxes: low residue flux (LRF) and water soluble flux (WSF); four different alternate surface finishes (ASFs); benzimidazole, immersion Ag, immersion Au/Pd, and HASL with solder mask. Furthermore the test samples were subjected to combinations of two simulated test exposures.

The adhesion test samples also include the effects from the environmental exposures. These were CA followed by thermal cycling from –60°C to 100°C for 500 + cycles with a ramp rate of 5°C /minute and dwell time of 30 min at each temperature extreme. The 85/85 test samples were subsequently subjected to 200 cycles of thermal shock in which samples were alternated between hot and cold chambers maintained at +125°C and –50°C with a 30-min dwell at each temperature extreme. The other population of test samples was exposed to diesel fluid followed by hydraulic fluid.

5.2.3 Adhesion Test Procedure

The Adhesion Test Method used was ASTM D-3359 – 97, Method B

Number of Tests: One crosshatch test per sample in customer specified location

Scribing Tool: Single edge razor blade,
1.0 mm blade spacing for Parylene,
2.0 mm blade spacing for Urethane

Tape: Permacel Brand 99 (ACT Labs Inc. catalog # 286) for Parylene and Urethane

Adhesion Rating Scale:

- 5B – The edges of the cuts are completely smooth; none of the squares of the lattice is detached.
- 4B – Small flakes of the coating are detached at intersections.
- 3B – Small flakes of the coating are detached along the edges and at intersections of cuts
- 2B – The coating has flaked along the edges and on parts of the squares
- 1B – The coating has flaked along the edges of cuts in large ribbons and whole squares have detached.
- 0B – Flaking and detachment worse than Grade 1.

Evaluation: Adhesion rated under UV light using a 7X magnifier

UV light/radiation: Macbeth light booth (ACT Labs Inc.catalog # 61)

5.2.4 Deviations From the Joint Test Protocol

For the silicone coated CCAMTF Test vehicles the tape peel test portion of the adhesion test could not be performed. While the scribing process development was successful, the test tape would not adhere to the silicone coating. Tapes currently manufactured have either acrylic adhesive or weak silicone pressure sensitive adhesives. Neither tape would adhere to the silicone surface even after applying the required thumbnail pressure and/or using an orange stick. It was impossible then to generate any useful data that would indicate the silicone coating's adhesion qualities in the same manner as for all the other coatings, and whether there were any distinguishable similarities or differences based on flux, coating and/or environmental test. Instead an alternate method of visually inspecting the coated surfaces of the assembly was performed to see if there were any differences in the coating adhesion. Optical observations between 4X and 10X were made and reported as separate data.

5.2.5 Adhesion Testing Results – ASTM D 3359

The adhesion test data is compiled from the raw data that was reported by ACT Labs Inc. on the CCAMTF test vehicles and was sorted as follows in Appendix E, as provided by Raytheon Electronic Systems, El Segundo, California:

This test data is only from Parylene and Urethane conformal coated test vehicles. The data includes all test samples for Phase I and II / Test Increments II & III & IV as described in the initial Scope and modified Statement of Work (SOW).

In this discussion, the silicone conformal coated test vehicles are not included as mentioned in Section 4.5.3. This is because a tape could not be found among those currently existing in the industry that had sufficient adhesion strength to a silicone coated surface to perform the requisite peel back/pull portion of the adhesion test. Therefore, it was determined that the silicone vehicles would be inspected visually and observations made in the different area of the Conformal Coated Assemblies (CCA) by component type, substrate, and solder joint type.

5.2.6 Data Analysis Sort by Surface Finish

A cursory inspection of the rating data showed that the surface finish when combined with either coating Parylene, or urethane typically yielded a rating of “5B” with Failure Level - None. When flux type was added, the ratings were similar. However, when combined with test condition type, there was some variation in the data. The accelerated life test condition resulted in a few ratings ranging from 2B to 4B with a failure level in the “substrate to topcoat.” There was one anomalous set of data in which the test vehicles with silver finish, processed with LR flux, and with a conformal coating of urethane and subjected to accelerated life test conditions yielded a 2B in one instance and 4B in another. The reason for this data is unknown but could be attributed to test technique.

5.2.7 Data Analysis Sort by Coating Type

Almost all the Parylene sorted adhesion test data had a “5B” rating and failure level of “none”, regardless of surface finish type, flux, and test condition exposure type. Visually the Parylene coated modules were unchanged from the as-coated condition prior to test exposure. See figure 3A in Appendix E for an example of Parylene coated module

Again there was some variation among the urethane coated adhesion test data. Most of these CCAs gave a “5B” rating. However, when combined by testing type, there was significant difference in the resultant adhesion test data. Almost all the urethane coated CCAs when subjected to condensing moisture (CM) and subsequent SF, gave a “0B” rating even for all surface finishes and fluxes. Corrosion can be observed underneath the

urethane coating of most of these samples. Figure 3B and Figure 3C in Appendix E are photo examples of test vehicles coated with urethane before and after condensing moisture and salt fog exposure respectively.

The accelerated life variable coupled with urethane conformal coating combination also gave some lower ratings for two of the samples and a moderate rating of “4B” for seven to eight of the CCAs tested. This variation in the data is most likely due to operator test technique.

5.2.8 Data Analysis Sort by Flux Type

This group gave the most varied data ratings and requires a more extensive data analysis tool to see if there are any trends.

5.2.9 Data Analysis Sort by Test Conditions

The test conditions used to sort were defined as follows – “CM/SF” for condensing moisture followed by salt fog, “Acc Life” for accelerated life, “DF” diesel fluid followed by “HF” hydraulic fluid, 85/85/TC for 85°C /85 % relative humidity followed by TS, “CA” for condensing atmosphere followed by TC. Each assembly was subjected to two rounds of testing: either all environmental, one environmental and one reliability, or all reliability testing. For accelerated life test vehicles, they were also exposed to vibration testing, mechanical shock, and condensing moisture.

In this sub grouping, the adhesion test data showed that most of the Parylene coated test vehicles did not differ significantly according to any of the environmental or reliability test exposures.

The adhesion data for the Urethane coated CM/SF tested assemblies yielded a “0B” rating with failure levels of “substrate to topcoat” for most of the modules tested. This subpopulation also included all surface finishes and flux types evaluated. The second significant test condition that impacted the adhesion test-rating outcome was accelerated life. However this data shows a wider range of results and requires sub grouping either by flux type and/or surface finish to determine whether there is some effect from these parameters.

5.2.10 Silicone Coating Results

Optical inspection between 4 and 10 power magnification of representative silicone modules with visual and UV light showed that each sub population differed in appearance depending on the environmental test parameters and surface finishes. Two modules that were inspected were subjected to either acidic salt fog or thermal humidity cycling. There was definite indication of corrosion on the various metallized areas, such

as the solder joints and traces. In the flat surface areas the coating was thin over the plated up metallized conductors. These areas exhibited slight corrosion or rust like appearance. These areas were also probed gently with an orange stick. The coating material was very susceptible to gentle abrasion after exposure, possibly an indicator that the coating material had degraded. Under UV, these metal areas did not fluoresce indicating that the coating material did not wet these areas. This was also evident on the backside (solder joint side). This was consistent for either leaded or non-leaded components.

There were two other modules that appeared to also exhibit similar characteristics except the surface finish was either an organic solder preservative (OSP) or bare copper. The coating's ability also appeared to have reduced protection as seen by visual evidence of easily being abraded. Also along the edges of the CCA, there was coating noticeably absent that probably was there before environmental exposure. Gentle probing of these areas showed that the coating material separated from the board with ease.

Two other boards did not show any physical changes to the board surface conductors or component bodies, solder joints and had metallized surface finish appearance possibly either Sn/PB HASL or immersion silver. These test vehicles could have been hydraulic or diesel fluid exposed and did not seem to show any signs of irreversible swelling or blistering. Silicones are known to not be as fluid resistant as their fluorosilicone counterparts when inspected immediately after fluid exposure. But since these modules had been separated from any fluid contact for an appreciable amount of time, any indications of swelling probably had disappeared.

It seems difficult to generalize the visual equivalent of the adhesion test based on the sample count inspected. Of those visually inspected, the one common observation among all three sample types was the silicone conformal coating's ability to achieve uniform edge and point coverage over solder joint tips of through hole solder joints. Also most of the silicone-coated vehicles that were visually and optically examined showed considerable evidence of corrosion along conductors and solder joints underneath the coating. The coating in these areas indicated a weakened physical appearance when probed or gently abraded and was typical for test vehicles exposed to some form of combined thermal moisture cycling and salt fog. Other than that there are unique but subtle differences among the sub-population of boards. A larger quantity of visual inspections would be needed to see if there are any correlations that exist between the various hardware and process variables.

6.0 CONCLUSIONS

The key HazMats that were to be addressed in this project were VOCs that are emitted into the environment during the application of conformal coatings and lead waste and exposure risks associated with the surface finishes applied to PWAs.

Upon completion of the rigorous testing matrix, which has been described and outlined in the previous sections, the CCAMTF found only isolated instances where surface finish was a significant factor in circuit performance. The results obtained and summarized in this report shows little difference in almost all cases and test sequences. Therefore, all surface finishes that were evaluated appear to be viable choices. However, the CCAMTF recommends that any decision by the reader regarding modifications to materials or processes should be supported by confirmatory tests conducted on specific products and environments.

The summary in Table 11 gives the average number of anomalies per PWA by conformal coating status for portions of each of the five groups of test environments. Nine of the 14 cases (DF, HF, Post BW, 85/85, TS, TC, AL, Vib, MS) and possibly the second listing of Post BW showed that conformal coating provided little, if any, improvement in performance and as such, are probably not cost effective in these environments. However, some types of conformal coating clearly helped in some test sequences (BW Vertical, SF, Cycle 10), but they did not necessarily prove to be a panacea for these environments.

Table 11. Average Number of Anomalies by Coating Status for Portions of the Five Test Sequences

Test Sequence	Uncoated	Parylene	Silicone	Urethane	
1	DF	0.05	0.33	0.08	0.10
	HF	0.05	0.18	0.03	0.10
2	BW Vert	11.65	8.20	7.90	8.25
	Post BW	0.68	0.20	0.13	0.25
	SF^{1, 2}	11.20	8.30	7.10	9.28
3	85/85	0.43	0.13	0.15	0.13
	200TS	0.30	0.20	0.15	0.20
4	Cycle 10	5.63	1.15	0.85	2.93
	500TC	0.15	0.15	0.25	0.20
5	AL	0.18	0.10	0.18	0.15
	Vib	0.40	0.23	0.25	0.30
	MS	0.53	0.20	0.25	0.18
	BW Vert	7.00	4.73	6.78	6.08
	Post BW	1.05	0.25	0.58	0.53
	Averages	2.75	1.73	1.76	2.06

¹ The reader is cautioned to fully review the complete test results contained in the appendix of this report prior to making process changes, or implementing any of the technologies discussed in this report.

² A full review of the deviations, Section 2.5, should be conducted regarding the salt fog data contained herein.

For example, during the BW vertical position in the BW-SF test sequence every PWA had at least four anomalies. Table 11 shows that coated PWAs have an average of approximately three less anomalies per PWA at BW vertical in the BW-SF test sequence, but they all have an unacceptably high level of anomalies. Hence, coating did not provide a satisfactory level of performance. Following SF, parylene (8.30) and silicone (7.10) have lower averages than uncoated (11.20) and urethane (9.28), but again coating still does provide a satisfactory level of performance in this extreme environment. Note that uncoated and urethane have almost the same averages after SF.

During Cycle 10 of the CA-TC test sequence parylene and silicone both lead to improvement in circuit performance, as does urethane to a lesser extent. Parylene is slightly better during the BW vertical test in the AL-Vib-MS-BW test sequence, but silicone and urethane are both very similar to the uncoated group. The overall averages given in the last row show that uncoated PWAs have approximately one more anomaly than parylene and silicone, and about 0.6 anomalies higher than urethane.

The PWAs were tested at the end of the 83 cycle of SF. However, after one week (168 hr) of SF testing, two members of the CCAMTF, one of who is an experienced corrosion specialist, performed a physical examination of the PWAs. It was their opinion that all specimens except for the parylene-coated PWAs had so much corrosion that they were considered to have essentially failed at that time. Uncoated specimens were by far the worst at this point. After examination at the end of 500 hr of SF exposure, there was more corrosion on all specimens except for the parylene-coated specimens. Their conclusion was that the parylene-coated specimens were the only specimens that were corrosion free. Moreover, any electrical anomalies recorded for the parylene PWAs were more likely the result of corrosion of the electrical connections, the test equipment or hidden parylene voids. Their reasoning for this is the pristine appearance of the observable surfaces and the corrosion spots and salt deposits on the unprotected contacts that could obviously provide resistance during the testing. (The technician tried to clean up the contacts but this did not always give the desired results.) The obviously corroded appearance of the non-parylene coated boards after salt fog gave strong evidence of the protection of the parylene.

Electrical testing was quite difficult after the SF test as the connectors were corroded (the JTP test protocol did not specify that the connectors should be masked) on all PWAs, which undoubtedly affected the test results. Uncoated PWAs arced during the HVLC and current leakage testing, and the HF tests showed abnormal waveforms. In addition, the ammeter over ranged or could not stabilize during many of the tests, which created unstable readings. Due to these concerns, anomalous measurements were not retested after SF as they were in all other stages of the CCAMTF test program. Not surprisingly, there were a large number (1435) of anomalies. In fact, every PWA had at least two anomalies and the median number of anomalies was 9. The uncoated PWAs had an average of 11.2 anomalies per PWA while the coated PWA had the following averages: parylene (8.3), silicone (7.1), and urethane (9.3). Statistical analysis shows that uncoated PWAs had significantly more anomalies than coated PWAs. Likewise, urethane coated

PWAs had significantly more anomalies than silicone coated PWAs, but not more than parylene. Parylene and silicone were not significantly different, though silicone averaged 1.2 less anomalies than parylene. Due to this large level of corrosion it should be noted that the salt fog test might be too severe of a test when evaluating the level of PWA performance.

Some differences were detected in flux types that were applicable to specific circuits in specific environments. These differences were too unpredictable to make generalizations. Please see Appendix E for specific details.

During the adhesion tests it was found that parylene coated test vehicles yielded high ratings for those that were tested. The results showed very little differentiation between flux type, alternative surface finish type and the environmental/reliability test combinations. Overall the Parylene coating yielded the highest level of adhesion.

The Urethane coated PWAs yielded high ratings for the adhesion testing until the condensing moisture/salt fog test combination. For this combination of exposures the Urethane coating yielded the lowest possible ratings with respect to adhesion.

The urethane coated PWAs also performed poorly with respect to adhesion following the accelerated life test. Although these ratings were not as low as those obtained during the condensing moisture/salt fog they were not in the acceptable range.

As noted in Section 5.2.4 the Silicone coated PWAs could not be tested using the ASTM D3359 tape test procedure. This inability to perform the noted testing procedure was due to a lack of test tape with sufficient adhesive strength capable of adhering to silicone coated surfaces. Due to this lack of an appropriate tape an optical inspection was required to be performed in place of the ASTM D 3359 standard. This inspection showed visual evidence of the silicone coating being less adherent over conductors and solder joints that showed corrosion. Visual inspection under UV exposure showed that the silicone coating had reduced edge and point coverage along component board edges and solder joints.

7.0 REFERENCES

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- “Joint Test Protocol, CC-P-1-1, for Validation of Alternatives to Lead-Containing Surface Finishes, for Development of Guidelines for Conformal Coating Usage, and for Qualification of Low-VOC Conformal Coatings”, Engineering and Technical Services for Joint Group on Acquisition Pollution Prevention (JG-APP), Contract No. DAAA21-93-C-0046, Task No. N.072, CDRL No. A005March 11, 1998, (Revised June 23, 1999)

8.0 ACRONYMS

Table 12 contains the acronyms used in the JTR

Table 12. Acronyms

Acronym	Definition
A	Amperes
ACI	American Competitive Institute
AF	Air Force
AFB	Air Force Base
AFMC/LG-EV	Air Force Materiel Command/Logistics Group - Environmental
Ag	Silver
Ag/Pd	Silver/Palladium
AL	Accelerated Life
AL-Vib-MS-BW	Accelerated Life, Vibration, Mechanical Shock, and Branch Water
AMCOM	Army Aviation and Missile Command
AMRAAM	Advanced Medium Range Air-to-Air Missiles
ASC/EM	Aeronautical System Center/Environmental Management
ASF	Alternate Surface Finish
ATAS	Advanced Tank Armament System
ATS	Automated Test Set
Au	Gold
Au/Pd	Gold/Palladium
BW	Branch Water
CA	Condensing Atmosphere
CCA	Conformal Coated Assemblies
CCAMTF	Circuit Card Assembly and Materials Task Force
CECOM	Communications Electronics Command
CM	Condensing Moisture
CNO	Chief of Naval Operations
CTC	Concurrent Technologies Corporation
CTE	Coefficient of Thermal Expansion
DCMA	Defense Contract Management Agency
DCMDW-OS	Defense Contract Management District – West
DEPTH	Design, Evaluation for Personnel, Training, and Human Factors
DF	Diesel Fuel
DoD	Department of Defense
EOS	Electrical Overstress
ESOH	Environmental, Safety, and Occupational Health
ESSM	Evolved SeaSparrow Missile
FOD	Foreign Object Debris
g	Gram

(Table 13 continued on next page)

Table 13. Acronyms (continued)

Acronym	Definition
GMLS	Guided Missile Launching System
GPSLOS	Gunner's Primary Sight-Line of Sight
HASL	Hot Air Solder Leveling
HazMats	Hazardous Materials
HCLV	High Current, Low Voltage
HF	High Frequency
HF	Hydraulic Fluid
HPM SEAD	High Power Microwave Suppression of Enemy Air Defenses
HQ	Head Quarters
Hr	Hour
HSD	High Speed Digital
HTI	Horizontal Technology Integration
HVLC	High Voltage, Low Current
IBAS	Improved Bradley Acquisition System
ITAS	Improved Target Acquisition System
ITSGMS	Integrated Targeting System Gun Management System
JASSM	Joint Air To Surface Standoff Missile
JG-PP	Joint Group on Pollution Prevention
JLC	Joint Logistics Commanders
JSF	Joint Strike Fighter
JSOW	Joint Stand Off Weapon
JTP	Joint Test Protocol
JTR	Joint Test Report
JWG	JG-PP Working Group
lbs/gal	Pounds per Gallon
LEAP	Lightweight Exo-Atmospheric Projectile
LPF	Low Pass Filter
LR	Low Residue Flux
LRF	Low Residue Flux
LRSTF	Low-Residue Soldering Task Force
MACOM	Major Command
Min	Minute
MS	Mechanical Shock
N/A	Not Applicable
NA	Not Available
NASA	National Aeronautics and Space Administration
NAWC	Naval Air Warfare Center
NDCEE	National Defense Center for Environmental Excellence
NDCEE/CTC	National Defense Center for Environmental Excellence/Concurrent Technologies Corporation

(Table 13 continued on next page)

Table 13. Acronyms (continued)

Acronym	Definition
NSWC	Naval Surface Warfare Center
OEM	Original Equipment Manufacturere
OICW	Objective Individual Combat Weapons
ON	Other Networks
OSP	Organic Solder Preservative
PSA	Pressure-Sensitive Adhesive
PTH	Plated Through Hole
PWA	Printed Wiring Assembly
RAM	Rolling Airframe Missile
RH	Relative Humidity
SAR	Synthetic Aperture Radar
SF	Salt Fog
SHORAD	Short-Range Air Defense
SMT	Surface Mount Technology
Sn/Pb	Tin Lead
SOW	Statement of Work
SPAR	Solid-State Phased Array
SVML	Standard Vehicle Mounted Launcher
STAFF	Smart Target Activated Fire and Forget
SW	Stranded wire
TACOM	Tank-Automotive and Armament Command
TADS/PNVS	Target Acquisition Designation Sight/Pilot Night Vision Sensor
TBIP	Tomahawk Baseline Improvement Program
TC	Thermal Cycle
TLC	Transmission Line Coupler
TS	Thermal Shock
TUAV	Tactical Unmanned Air Vehicle
Vib	Vibration
VOC	Volatile Organic Compound
WSF	Water Soluble Flux
WR-ALC	Warner Robins Air Logistics Center

APPENDIX A

Participating CCAMTF Organizations and Representatives

Table A-1. Participating CCAMTF Organizations and Representatives

Organization	Representative	OEM Type
Alliant Techsystems	Mark Shireman, (612) 931-6506	Military
Allied Signal - Kansas City Division	Gary Becka, (816) 997-4542	Government
Boeing	Willy Chang, (253) 657-9194	Commercial
Contamination Studies Laboratory, Inc.	Terry Munson, (765) 457-8095	Commercial
Electronic Manufacturing Productivity Facility	Mike Czajkowski, (610) 828-8100	Military
Hughes Space & Communication	Tom Carroll (310) 334-4757	Military
GTE	Bill Hubbard, (508) 880-1793	Military
Hanscom AFB	Chuck Bowers (617) 377-8143 Tom Thornton (617) 377-8138	Military
Honeywell	Tom Lepsche, (505) 828-5396	Military
Les Hymes Associates	Les Hymes, (541) 687-0011	Commercial
Lucent Technologies	George Wenger, (609) 639-2769 Bruce Stacy, (908) 582-4289	Commercial
Lockheed Martin Electronics and Missiles	John Lampe, (407) 356-7103 Linda Dolan, (407) 356-2520	Military
Lockheed Martin Tactical Aircraft Systems	Tony Phillips, (817) 777-3758 Charles Palermo, (817) 777-4014	Military
Motorola	Prasad Godavarti, (512) 933-7636	Commercial
Robisan Laboratory	Susan Mansilla, (317) 353-6249	Commercial
Rockwell Collins	David Hillman, (319) 295-1615	Military
Southwest Technology Consultants	Ronald L. Iman, (505) 856-6500	Commercial

(Table A-1 continued next page)

Table A-1. Participating Organizations and Representatives (Continued)

Organization	Representative	OEM Type
Raytheon Systems Company	Jeffry F. Koon, (972) 952-4434 Samantha Walley, (310) 334-3794 Jim Reed, (512) 250-7172 Mike Leake, (972) 334-2071 Jeff Bradford, (972) 952-2170 Mahendra Gandhi, (310) 616-3151 Fonda Wu, (310) 334-3636	Military
US Army - AMCOM, Huntsville	David Carlton, (205) 876-9744	Military
US Army - Picatinny	Larry Genereux, (201) 724-7319	Military
ViaSystems	Lee Parker, (804) 226-5402	
Wright-Patterson AFB	Max Delgado, (937) 255-3059 X329	Military

APPENDIX B

**Low Residue Soldering Task Force (LRSTF)
Printed Wiring Assembly (PWA)**

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B.1 DESIGN OF THE LOW RESIDUE SOLDERING TASK FORCE (LRSTF) PRINTED WIRING ASSEMBLY

The primary test vehicle used in the LRSTF evaluation of low-residue technology was an electrically functional printed wiring assembly (PWA). This assembly was designed at Sandia National Laboratories in Albuquerque, NM based on input from LRSTF members and input received during open review meetings held by the task force.

The PWA measures 6.05 inches x 5.8 inches x 0.062 inches and is divided into seven sections, each containing one of the following types of electronic circuits:

- High Current, Low Voltage (HCLV)
- High Voltage, Low Current (HVLC)
- High Speed Digital (HSD)
- High Frequency Low Pass Filter(LPF)
- High Frequency Transmission Line Coupler (TLC)
- Other Networks (ON)
- Stranded Wire (SW).

The layout of the LRSTF functional assembly is shown in Figure B-1. Each quadrant of the PWA has subsections for PTH and SMT components, with each forming separate electrical circuits. The PWA includes a large common ground plane, components with heat sinks, and mounted hardware.

Each subsection shown contains both functional and nonfunctional components (added to increase component density). A 29-pin PTH edge connector is used for circuit testing. High frequency connectors are used to ensure proper impedance matching and test signal fidelity as required. Board fabrication drawings, schematics, and a complete listing of all components are available in separate cover.

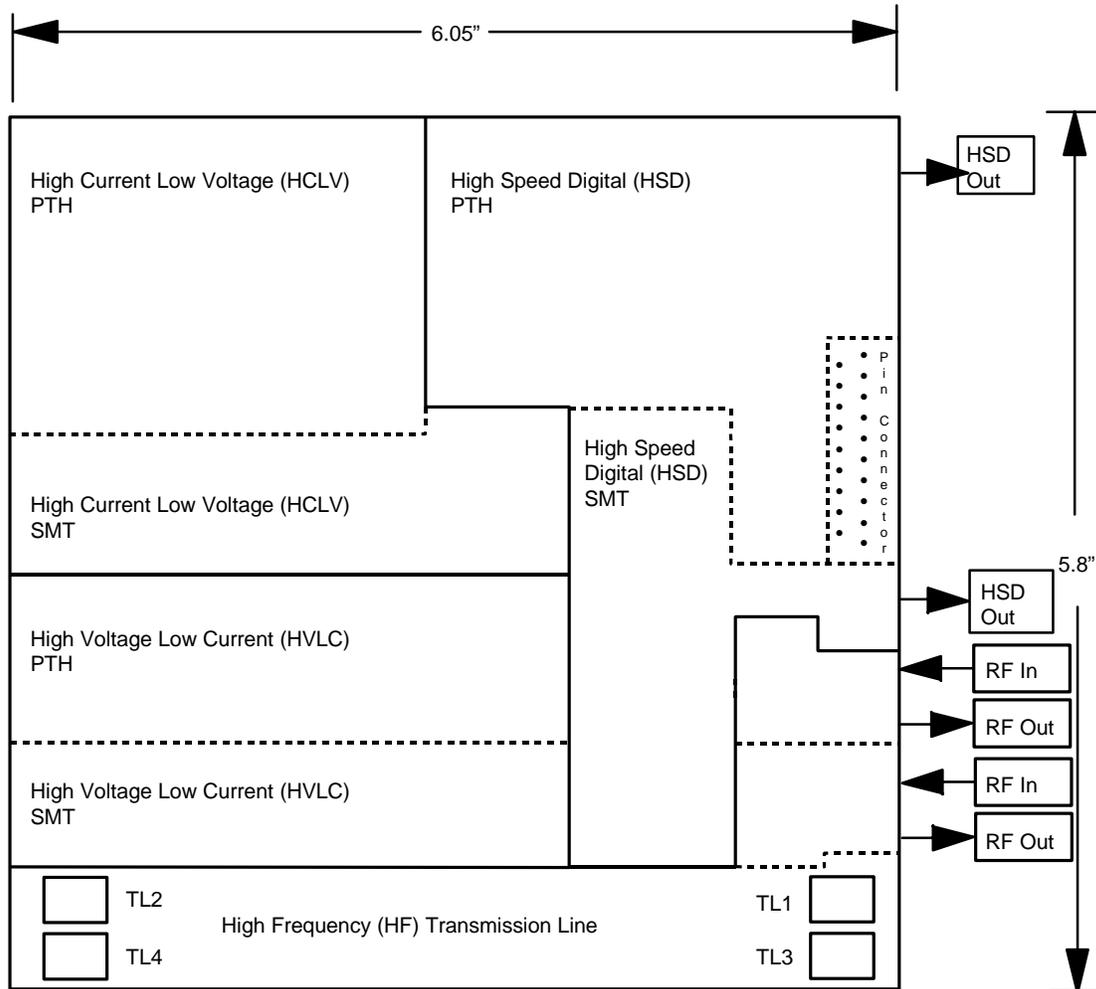


Figure B-1. Layout of the PWA Illustrating the Four Major Sections and Subsections

B.2 HIGH CURRENT, LOW VOLTAGE (HCLV)

The HCLV section of the board is in the upper left-hand corner of LRSTF PWA (see Figure B-1). The upper left-hand portion of this quadrant contains PTH components with SMT components immediately beneath.

Purpose of the HCLV Experiment

Performance of high-current circuits is affected by series resistance. Resistance of a conductor (including solder joints) is determined by the following equation:

$$R = \frac{\rho L}{A_c} \text{ ohms}(\Omega) \quad (\text{B.1})$$

where ρ = resistivity, the proportionality constant
L = length of the conductor
 A_c = cross-sectional area of the conductor (solder joints).

Resistance is most likely to change due to cracking or corrosion of the solder joint that may be related to the soldering process. These conditions decrease the cross-sectional area of the solder joints, thus increasing resistance as shown in Equation B.1. Use of high current to test solder joint resistance makes detection of a change in resistance easier.

A 5 Amperes (A) current has been selected as a value that would cover most military applications. A change of resistance is most conveniently determined by measuring the steady-state performance of the circuit, which will now be discussed.

Steady State Circuit Performance.

Overall circuit resistance, R_{total} , is the parallel combination of the seven resistors, R_1 ,

R_2, \dots, R_7 , (all resistors = 10Ω) used in the HCLV circuit:

$$\frac{1}{R_{total}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_2} + \dots + \frac{1}{R_7} = \frac{7}{10\Omega} \quad (\text{B.2})$$

$$R_{total} = \frac{10\Omega}{7} \quad (\text{B.3})$$

Since a current (I) of 5A will be applied to the circuit, the resulting voltage (V), according to Ohm's Law, is:

$$V = IR = 5A \times \frac{10\Omega}{7} = 7.14V \quad (\text{B.4})$$

Changes in resistance are thus detected by changes in voltage. However, a pulse width had to be chosen that would not overstress the circuit components. With current equally divided among the seven parallel resistors, the power (P) dissipated in each resistor, according to Joule's Law, is:

$$P = I^2 R = \left(\frac{5A}{7}\right)^2 \times 10\Omega = 5.1Watts(W) \quad (B.5)$$

Since the power rating for the PTH wire-wound resistor is 3W, the rating is exceeded by a factor of 1.7 for steady state (5.1 / 3). Design curves from the resistor manufacturer indicate the PTH wire-wound resistors could tolerate the excess power for about 100 ms. The SMT resistors are rated at 1W, so the steady state rating is exceeded by a factor of five. With the manufacturer unable to provide the pulse current capability of the SMT resistors, a pulse derating factor could not be determined. A pulse width of 100 μs was selected, which is three orders of magnitude less than the capability of the wire-wound resistors. This width is also sufficiently long for the circuit to achieve steady state before the measurement is taken.

Circuit Board Design

Traces carrying the 5A current were placed on an inner layer of the circuit board because: (1) the primary concern was the possible degradation of the solder connections as discussed above, and (2) the bulk electrical characteristics (resistivity) of the traces should not be affected by flux residues. High-current trace widths were designed to be 250 mils whenever possible (following MIL-STD-275). This width with a 5A current should cause no more than a 30°C temperature rise under steady-state conditions.

The resistor and capacitor values were selected to be readily available. If other values are used, care should be taken to not over-stress the parts, as discussed above.

B.3. HIGH VOLTAGE LOW CURRENT

The HVLC circuitry is immediately below the HCLV circuitry and above the high-frequency transmission lines. The PTH circuitry is in the upper part of this subsection with the SMT circuitry beneath.

Purpose of the HVLC Experiment

Flux residues could decrease the insulation resistance between conductors. The impact of this decrease could be significant in circuits with a high-voltage gradient across the insulating region. Decreased resistance can be detected by an increase in current when a high voltage is applied to the circuit. A voltage of 250V was selected as the high potential for this test. The change in leakage current is determined by measuring the steady-state performance of the circuit, which will now be discussed.

Steady State Circuit Performance

Steady-state operation of the HVLC circuit can be determined by considering only the resistors. The total resistance of the series combination is the sum of the resistances:

$$R_{total} = R_1 + R_2 + R_3 + R_4 = R_5 = 50M\Omega \quad (B.6)$$

since all resistors are 10M Ω each.

From Ohm's law, the current flowing into the circuit with 250V applied is:

$$I = \frac{V}{R} = \frac{250V}{50M\Omega} = 5\mu A \quad (B.7)$$

Care was taken to not over-stress the individual components in the circuits. The voltage stress across each resistor-capacitor pair is one-fifth of the applied 250V, or 50V. The voltage ratings are 250V for the PTH resistors, 200V for the SMT resistors, and 250V for all the capacitors. Power rating is not a concern due to the low current.

Circuit Board Design

High voltage traces were placed next to ground potential traces by design. The spacings between the high voltage and intermediate traces were selected using MIL-STD-275 and were calculated as shown in Table B-1 below.

Table B-1. Voltage per Trace Spacing

Voltage	Spacing Between Traces (mils)
0 - 100	5
101 - 300	15
301 - 500	30

These guidelines were followed except the 5-mil spacing, where 10 mils was used to facilitate board fabrication. Table B-2 lists the voltage on various board circuit traces and the spacing to the adjacent ground trace.

Resistors and capacitors were selected to have readily available values — different values could have been used to achieve particular experimental goals. For instance, higher-resistance values could be used with lower-value capacitors. Reverse biased, low-leakage diodes could also be used for higher sensitivity to parasitic leakage resistance.

Table B-2. HVLC Circuit Board Trace Potentials

Technology	Trace Connected to:		Potential (V)	Trace Length at Potential (in)	Spacing (mils)
	Resistor	Capacitor			
PTH	R15	C21	250	0.8	30
			200	0.4	15
	R16	C22	200	0.4	15
			150	N/A	
	R17	C23	150	N/A	
			100	0.4	10
	R18	C24	100	0.4	10
			50	N/A	
	R19	C25	50	N/A	
	SMT	R20	C26	250	5.0
			200	1.0	15
R21		C27	200	1.0	15
			150	N/A	
R22		C28	150	N/A	
			100	0.9	10
R23		C29	100	0.9	10
			50	N/A	
R24		C30	50	N/A	

N/A = Not Applicable since no 50V or 150V traces were adjacent to ground potential

B.4. HIGH SPEED DIGITAL (HSD)

The HSD circuitry is in the upper right-hand corner of the LRSTF PWA as shown in Figure B-1. This subsection contains the PTH circuitry and consists of two 14-pin dual in-line package (DIP) integrated circuits (ICs). The SMT subsection IC is a single 20-pin leadless chip carrier (LCC) package. Each of these ICs is a “fast” bi-polar digital “QUAD-DUAL-INPUT-NAND-GATE.” Both subsections contain two ceramic capacitors that bypass spurious noise on the power input line (VCC) to the ICs and an output high-frequency connector. Inputs to both subsections are applied through the edge-connector on the right side of the board. Figure B-2 shows a simplified schematic of the ICs.

Purpose of the HSD Experiment

The output signal of each gate in Figure B-2 is opposite in polarity to the input signal. If the traces of these two signals are in close proximity on the printed circuit board (capacitively coupled), the gate switching speed might be affected by the presence of flux residues. A 5 VDC bias will be applied to the VCC inputs during environmental testing to accelerate aging. One PTH IC (U02) will be hand soldered during assembly at each site to introduce hand solder flux residue in the experiment.

Circuit Description

The schematic in Figure B-2 represents the ICs in the PTH and SMT subsections. The ICs are random logic circuits that are NAND (Not AND) gates. An AND gate’s output is high only when all inputs are high. The logic of a NAND gate is opposite the logic of an AND gate. Therefore, the output of a NAND gate is low only when all inputs are high; otherwise, the output is high. With the two connected inputs, the output of each gate is opposite the input. Since the four gates are connected in series, the output of the last gate is the same logic level (high or low) as the input, with a slight lag.

The output pulse does not change logic levels instantaneously, but the switching times from low to high (rise time) and from high to low (fall time) should be less than 7ns. ICs should perform within these criteria if the VCC input is $5 \pm 0.5V$ DC, the output load does not exceed specifications, and the circuit has a proper ground plane as shown in Figure B-2.

The HSD circuits also provide an intermediate test for high frequencies, with switching time dictating a high-frequency spectrum. The frequency spectrum of switching circuits can be expressed in terms of bandwidth (BW). For a switching circuit, the respective BWs (in Hertz) for rise (t_r) and fall (t_f) times are:

$$BW_r = \frac{0.35}{t_r} \text{ Hz} \quad \text{and} \quad BW_f = \frac{0.35}{t_f} \text{ Hz} \quad (\text{B.8})$$

Bipolar technology was used rather than a complementary metal oxide semiconductor (CMOS) since it is not as vulnerable to electrostatic discharge (ESD) damage. Available military bipolar technologies have typical switching speeds and bandwidths as indicated in Table B-3 below.

Table B-3. Typical Switching Speeds and Bandwidths

Technology	Typical t_r or t_f (ns)	Bandwidth (MHz)
5404 TTL	12	29
54LS04 Low Power Schottky	9	39
54S04 Schottky	3	117
54F04 Advanced Schottky (Fast)	2.5	140

The Fast technology was selected since it had the shortest switching time and largest bandwidth, which provides the widest frequency spectrum for this test.

Circuit Board Design

Ground planes were provided for proper circuit operation of the ICs. The PTH subcircuit utilized the large common ground plane on layer 3 since most of the input and output traces are on layer 4. Since the SMT circuit traces are on the top layer, a smaller ground plane was added on layer 2. The “QUAD-DUAL-INPUT-NAND-GATE” was selected since other solder studies of national attention have used that particular type of IC, which makes direct comparisons with these studies possible. See Figure B-2.

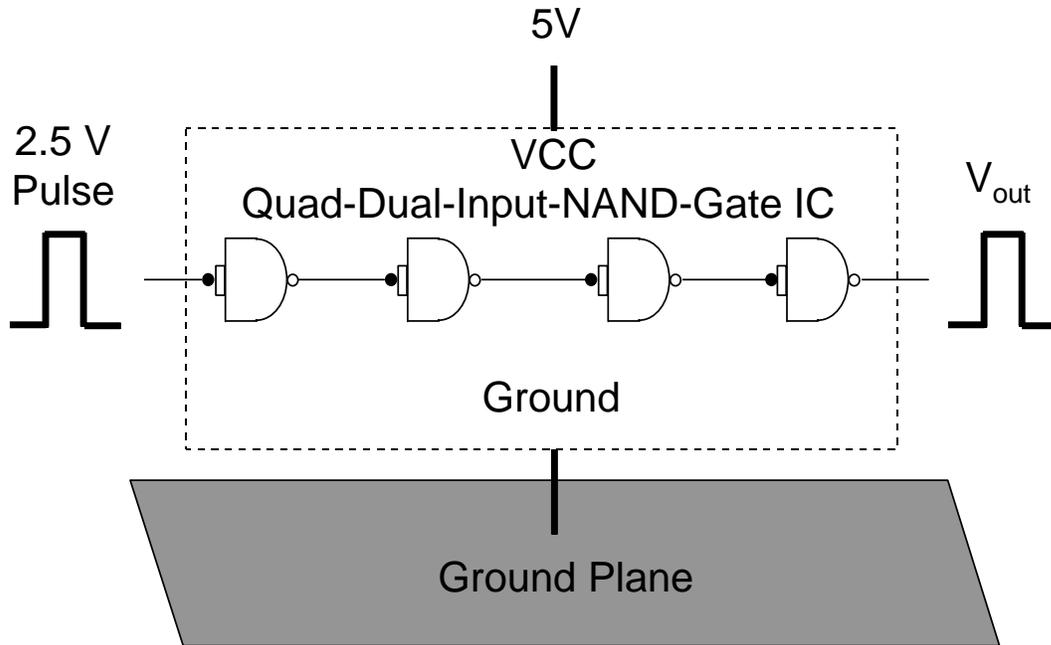


Figure B-2. Simplified Schematic of the ICs in the HSD Subsection

B.5. HIGH FREQUENCY (HF)

The HF section shown in the lower right-hand corner of Figure B-1 contains two major subsections, the low-pass filters (LPF) and the transmission line coupler (TLC). The TLC traces on layer 4 of the board are on the backside of the board. The LPF/PTH subsection is above the LPF/SMT subsection. Each of these subsections has discrete ceramic capacitors and three inductor-capacitor (LC) filters, with the inductor printed on the circuit board in a spiral pattern. The HF circuits allow evaluation of circuit performance up to 1GHz (1 GHz).

Purpose of the High Frequency Experiment

Flux residues may affect the performance of LPF printed circuit inductors and transmission lines due to parasitic resistances and parasitic capacitances. These inductors will be purposely covered with flux during surface-mount solder processing to increase the presence of residues. Since the transmission lines are separated by only 10 mils, flux residues between the lines may affect their performance.

LPF Circuit Description

An inductor-capacitor (LC) LPF consists of a series inductor followed by a shunt capacitor. A low-frequency signal passes through the LPF without any loss since the inductor acts as a short circuit and the capacitor acts as an open circuit for such signals. Conversely, a high-frequency signal is blocked by the LPF since the inductor acts as an open circuit and the capacitor acts as a short circuit for such signals.

When a sine wave test signal is passed through an LPF, its amplitude is attenuated as a function of frequency. The relationship between the output and input voltage amplitudes can be expressed as a transfer function. The transfer function, V_{out} / V_{in} , was measured to determine any effects of the low-residue fluxes.

The transfer function is measured in decibels (dB) as a function of frequency. A decibel can be expressed in terms of voltage as follows:

$$dB = 20 \log_{10} \left(\frac{|V_{out}|}{|V_{in}|} \right) \quad (B.9)$$

The PTH transfer function differs from the SMT transfer function due to the self inductance of the capacitor through-hole leads.

LPF Circuit Board Design

The three LC LPFs for each of the SMT and PTH circuits were designed to have the following cutoff frequencies: 800, 400, and 200 MHz. Cutoff frequency is

that frequency for which the transfer function is -3 dB. The respective component values chosen for the LC filters are 16 nH (nano-Henries) and 6.4 pF (pico-Farads), 32 nH and 13 pF, and 65 nH and 24 pF. Most LPF circuitry was placed on Layer 1, with Layer 2 used as a ground plane. Crossovers needed to connect the LPF circuits are on Layer 4.

The LPF circuits were designed to operate with a 50Ω test system, so all interconnect traces longer than 0.10 inches were designed as 50Ω transmission lines to avoid signal distortion. The LPF circuits were predicted to have less than 2 dB loss below 150 MHz, approximately 6 dB loss near 235 MHz, and greater than 40 dB loss at 550 MHz and beyond. The measured response of the LPF/SMT circuit is close to that predicted except that the transfer function decreases more rapidly than predicted above 350 MHz. As stated previously, the PTH circuit transfer function did not perform similarly to the SMT, particularly at frequencies above 150 MHz.

TLC Circuit Description

Figure B-3 shows a diagram of the TLC subsection. The LPFs described above are *lumped-element* circuits since the capacitors are discrete components. The TLC lines are *distributed-element* circuits with the resistors, inductors, and capacitors distributed along the lines. A circuit model for the lines is shown in Figure B-4.

The inductance and capacitance for a transmission line with a ground plane are, respectively:

$$L_L = 0.085R_0\sqrt{\epsilon_r}nH / in \quad (B.10)$$

$$C_L = \frac{85}{R_0}\sqrt{\epsilon_r}pF / in \quad (B.11)$$

where R_0 = characteristic resistance and ϵ_r = dielectric constant of the board material.

The TLC R_0 was designed to be 50Ω for operation with a 50Ω test system. For FR-4 epoxy (board substrate material), L_L is about 9.6 nH/in and C_L is about 3.8 pF/in.

The TLC was tested with a sine wave signal similar to the one used in testing the LPFs.

The source resistance was 50Ω and the three output terminals were connected to 50Ω loads.

TLC Circuit Board Design

The transmission line coupler (TLC) circuit has a pair of coupled 50Ω transmission lines with required measurable performance frequencies less than 1 GHz. Layer 4 of the PWA was used to route the TLC circuit, with Layer 3 used as the ground plane. The TLC circuit is a 5 inches long pair of 0.034 inches wide 50Ω transmission lines spaced 0.010 inches apart. The circuit design incorporated the board dielectric constant of about 4.8 inches and the .020 inch spacing between copper layers. A computer-aided circuit design tool (Libra) was used to model the TLC circuit. Performance measured on a test PWA agreed very closely with the forward and reverse coupling predictions between 45 MHz and 1 GHz.

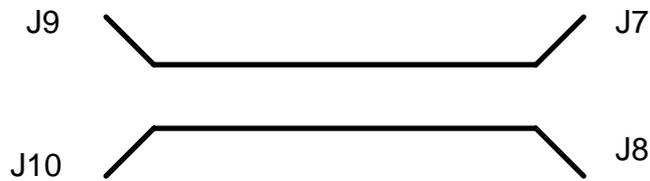


Figure B-3. Diagram of the HF/TLC Subsection

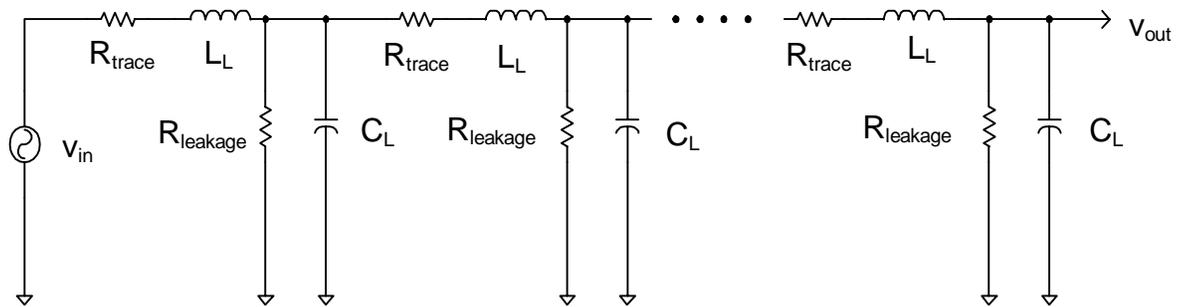


Figure B-4. HF/TLC Distributed Element Model

B.6. OTHER NETWORKS (LEAKAGE CURRENTS)

The LRSTF board also contains three test patterns to provide tests for current leakage: (1) the pin-grid array (PGA), (2) the gull wing (GW), and (3) 10-mil spaced pads. A 5 V source was used to generate leakage currents.

Purpose of the Experiments

The PGA, GW, and 10-mil pads allow leakage currents to be measured on test patterns that are typical in circuit board layouts. These patterns contain several possible leakage paths and the leakage could increase with the presence of flux residues and environmental exposure. In addition, solder mask was applied to portions of the PGA and GW patterns to evaluate its effect on leakage currents and the formation of solder balls.

Pin-Grid Array

The PGA hole pattern has four concentric squares that are electrically connected by traces on the top layer of the board as shown in Figure B-5. The pattern also has four vias just inside the corners of the innermost square that are connected to that square. Four vias were placed inside the innermost square to trap flux residues. Two leakage current measurements were made: (1) between the two inner squares (PGA-A) and (2) between the two outer squares (PGA-B), as shown in Figure B-5. Solder mask covers the holes of the two outer squares on the bottom layer, allowing a direct comparison of similar patterns with and without solder mask.

Rather than an actual PGA device, a socket was used since it provided the same soldering connections as a PGA device. Also, obtaining leakage measurements on an actual PGA is nearly impossible due to complexity of its internal semiconductor circuits.

Gull Wing

The upper half of the topmost GW lands and the lower half of the bottom most GW lands were covered with solder mask to create a region that is susceptible to the formation of solder balls. The lands were visually inspected to detect the presence of solder balls. A nonfunctional GW device is installed with every other lead connected to a circuit board trace forming two parallel paths around the device. Total leakage current measurements were made on adjacent lands of the GW device

10-mil Pads

The 10-mil pads were laid out in two rows of five pads each. The pads within each row were connected on the bottom layer of the board and leakage between the rows was measured.

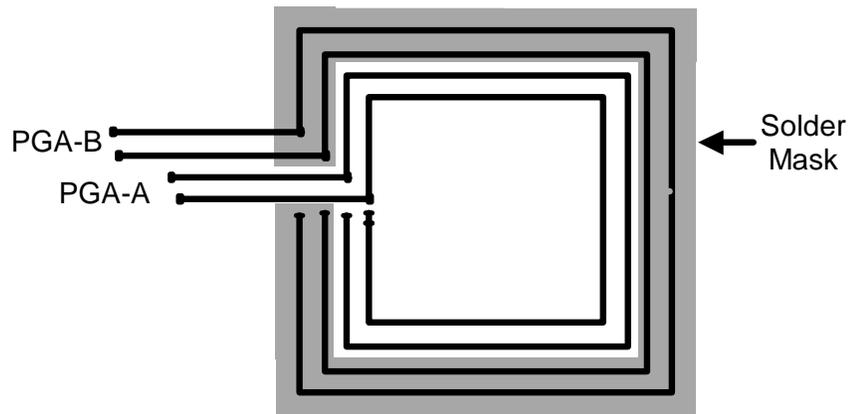


Figure B-5. PGA Hole Pattern with Solder Mask

B.7. STRANDED WIRES

Two 22-gauge stranded wires will be hand soldered just to the left of the edge connector. One wire will be soldered directly into the board through holes and the other will be soldered to two terminals, E17 and E18. Each wire is 1.5 inches long, is silver coated, and has white PTFE insulation. All wires will be stripped, tinned, and cleaned in preparation for the soldering process.

Purpose of the Stranded Wire Experiment

Stranded wires were used to evaluate flux residues and subsequent corrosion.

Circuit Description

The 5 A 100 μ s pulse used to test the HCLV circuit was injected into each of the stranded wires for electrical test. A separate PWA trace was connected to each end of the stranded wire. Test wires were connected to the separate traces allowing to provide the means to measure the voltage drop across the stranded wires. In this manner, the voltage drop was measured independently from any voltage drop in the test wires conducting the 5 A pulse to the stranded wires.

B.8. COMPONENTS

All functional component types conformed to commercial specifications and were ordered pre-tinned (to the extent possible). Components will not pre-cleaned before use.

Solderability testing will be performed using dip and look testing per MIL-STD-202, Method 208 with type R flux per MIL-F-14256. All functional components are required to pass solderability testing.

B.9. BOARDS

The four-layer LRSTF PWAs have exposed traces on both sides and will be manufactured to meet the requirements of MIL-P-55110. The substrate material will be FR-4 epoxy. Starting copper weight will be 1 oz/ft². An ionic cleanliness level of 5 or less $\mu\text{g}/\text{in}^2$ NaCl equivalence will be specified.



Figure B-6. LRSTF Functional Test Board

APPENDIX C

**Circuit Card Assembly and Materials
Task Force Automated Test Set
(ATS)**

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C.1. CCAMTF AUTOMATED TEST SET

The CCAMTF Automated Test Set (ATS) is used to perform automatic testing of the Low-Residue Soldering Task Force (LRSTF) printed wiring assembly (PWA). The Automated test set design was based on the original LRSTF manual test setup. The CCAMTF ATS was designed to emulate the LRSTF manual test set as much as possible. Some changes were made in the selection of commercial test equipment in order to facilitate the test software development process. Some test stimuli and test measurement techniques were also changed in order to be compatible with the commercial test equipment selected. See figure C-1.



Figure C-1. CCAMTF Automated Test Set

Table C-1. CCAMTF ATS Commercial Test Equipment

Test Equipment	Description
Hewlett Packard HP6289A	Power Supply
Hewlett Packard HP8112A	Pulse Generator
Hewlett Packard HP54111D	Digital Oscilloscope
Hewlett Packard HP6060B	Electronic Load
Hewlett Packard HP3488A	Switch/Control Unit (2 each)
Hewlett Packard HP44471A	General Purpose Relay (3 each)
Hewlett Packard HP44472A	VHF Switch(2 each)
Hewlett Packard HP44470A	10 Channel Relay Multiplexer
Hewlett Packard HP85046A	S - Parameter Test Set
Hewlett Packard HP8753A	Network Analyzer
Fluke 5700A	Voltage Calibrator
Keithley 617	Electrometer

The commercial test equipment is housed in a two bay cabinet. Signal routing and switching are performed by the HP3488 Switch/Control units. Custom designed interconnect cables are used to make the connections between the commercial test equipment, the switch/control units and the PWA under test. All commercial test equipment is connected to the computer using standard GPIB interconnect cables.

C.2. PWA TEST FIXTURE ASSEMBLY

The PWA Test Fixture Assembly contains interconnect wiring that provides electrical connection between the PWA under test and the commercial type test equipment as shown in Figure C-2 CCAMTF Automated Test Set PWA Test Fixture Assembly.

The PWA under test is mounted horizontally in the test fixture to facilitate the connection of RF coaxial cables. A cable harness is connected to the PWA edge card connector. Ejectors are provided to assist in the connector mating and demating. Two microwave coaxial switches are mounted in the base of the fixture. There are no other active components in the test fixture.

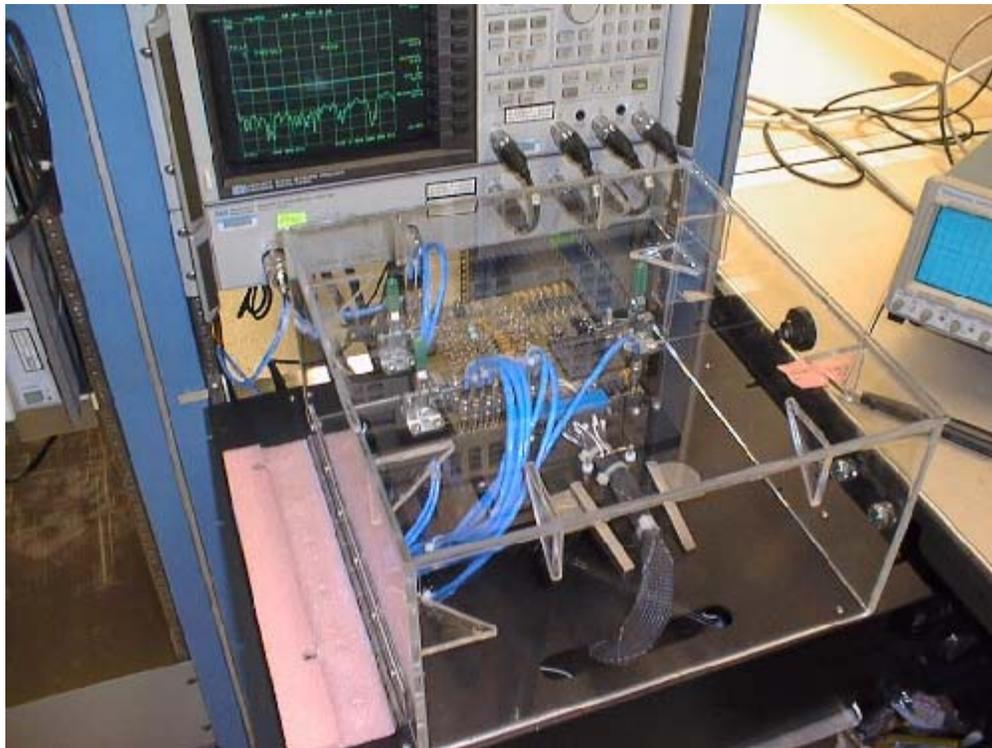


Figure C-2. CCAMTF Automated Test Set PWA Test Fixture Assembly

Two microwave switches provide signal switching for high frequency type measurements. One switch directs signals to the PWA inputs and the second switch selects the corresponding outputs that are routed to the measurement equipment. The coaxial switches are controlled by the computer and the test software. Coaxial cable insertion losses are measured during the ATS calibration procedure. Cable losses are recorded and subtracted from the PWA test measurements to arrive at the actual PWA insertion losses.

A plexiglas cover is provided to shield the operator from exposed high voltage on the PWA. An interlock switch is installed on the cover. Opening the cover will disconnect the high voltage from the PWA. Connections are provided on the plexiglas cover to attach a three inch flexible air hose. The air hose is connected to a facility exhaust system to prevent diesel and hydraulic fluid fume build up during the fluids testing procedure. The air hose connection is required only during the fluids test.

C.3. TEST SOFTWARE

An IBM compatible computer running the Windows operating system is used to control the test sequence and record test measurement results. Windows is a product of Microsoft Corporation, Portland, OR. A National Instrument GBIP Interface card is installed in the computer to interface with the commercial test equipment.

Test Executive (TEXEC) is a software system used to control test selection, test execution, and test data output. TEXEC is a product of Serendipity Systems, Inc. (SSI) of Sedona, AZ.

Lab Windows/CVI is a visual programming tool used to develop test software. Lab Windows/CVI is a product of National Instruments of Austin, TX.